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SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE
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SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE

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ABSTRACT

PURPOSE: To manufacture a high-performance and high-density large scale integrated circuit device with excellent yield by accurately aligning and laminating semiconductor layers whereupon a plurality of semiconductor integrated circuits are formed.

CONSTITUTION: A semiconductor integrated circuit device layer is formed by laminating a flat quartz substrate 30, which permeates ultraviolet rays, on the major surface of the semiconductor integrated circuit device formed on a semiconductor substrate with adhesive 20 and by thinning the layer. The thin layer and a separately prepared semiconductor substrate 11 mounted with a semiconductor integrated circuit device are aligned and laminated by high- accuracy using ultraviolet rays. An aligning device provided with a mechanism which corrects pattern deformation caused by film forming process, etc., in the whole area of the semiconductor substrate and allows correct aligning is used. After the second lamination, the first adhesive is melted so as to release the quartz substrate and a laminated semiconductor integrated circuit device is formed.

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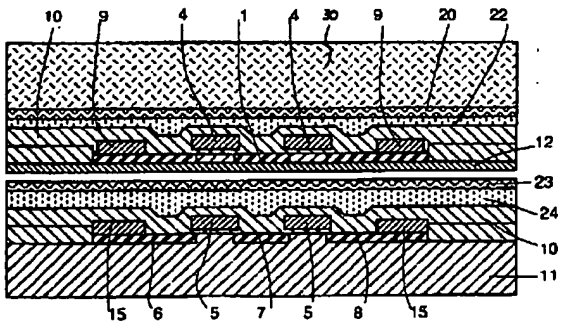
(54)【発明の名称】半導体集積回路装置及びその製造方法

(57)【要約】

【目的】　複数の半導体集積回路が形成された半導体層を高精度で位置合せして積層化することにより、高性能で高密度の大規模集積回路装置を歩留まり良く製造する。

【構成】　半導体基板に製造した半導体集積回路装置の主表面で紫外光を透過する平坦な石英基板３０と第１の接着剤２０により貼合せ、薄化により半導体集積回路装置層を形成する。上記薄層と別途準備した半導体集積回路装置が構成された半導体基板１１を紫外光を用いて高精度で位置合せし、貼合せる。成膜工程等で生じたパターン歪を半導体基板全領域で補正し、正確な位置合せを可能にする機構を付加した位置合せ装置を使用した。第２の貼合せ後、第１の接着剤を溶融して石英基板を剥離させ、積層半導体集積回路装置を形成する。

図7



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【特許請求の範囲】

【請求項１】絶縁膜で互いに分離された複数の単結晶半導体薄膜領域の各々に少なくとも一つの半導体装置が設けられ、且つ該半導体装置が配線層で互いに接続されてなる半導体集積回路装置層が積層化されて構成された半導体集積回路装置において、上記半導体集積回路装置層内にそれぞれ形成された半導体装置の一部は実質的に同一の伝達遅延時間特性を有し、且つ隣接する該半導体集積回路装置層間で互いに整合された半導体装置電極端子と、該端子を貫通して下部の該端子に達する接続導電体とを備えたことを特徴とする半導体集積回路装置。

【請求項２】絶縁膜で互いに分離された複数の単結晶半導体薄膜領域の各々に少なくとも一つの半導体装置が設けられ、且つ該半導体装置が配線層で互いに接続されてなる半導体集積回路装置層が積層化されて構成された半導体集積回路装置において、上記半導体集積回路装置層内にそれぞれ形成された半導体装置の一部は実質的に同一の伝達遅延時間特性を有し、且つ上層部の上記単結晶半導体薄膜領域を貫通して下層部の該単結晶半導体薄膜領域又は配線領域と接続される接続導電体を備えたことを特徴とする半導体集積回路装置。

【請求項３】請求項１又は２記載の半導体集積回路装置において、相接する上記半導体集積回路装置層は接着剤層を介さず直接貼合せにより積層化されていることを特徴とする半導体集積回路装置。

【請求項４】請求項１又は２記載の半導体集積回路装置において、上記半導体集積回路装置層はその上面および底面のいずれにも配線層を有することを特徴とする半導体集積回路装置。

【請求項５】請求項４記載の半導体集積回路装置において、上記配線層の少なくとも一層は面状であり、且つ電源電位、または接地電位を印加するための端子を有することを特徴とする半導体集積回路装置。

【請求項６】請求項１又は２記載の半導体集積回路装置において、相接する上記半導体集積回路装置層の一方には第一導電型半導体装置が、他方には第二導電型半導体装置が設けられ、互いに対をなすことを特徴とする半導体集積回路装置。

【請求項７】請求項１又は２記載の半導体集積回路装置において、相接する一方の上記半導体集積回路装置層の所望領域にはトランジスタが、他方の上記半導体集積回路装置層の所望領域には該トランジスタと整合して容量素子が設けられ、対をなすことを特徴とする半導体集積回路装置。

【請求項８】請求項７記載の半導体集積回路装置において、上記容量素子の一方の電極は高融点金属膜または高融点金属珪化膜と接続され、該金属膜または該金属珪化膜は上記トランジスタ下部に設けられていることを特徴とする半導体集積回路装置。

【請求項９】請求項１又は２記載の半導体集積回路装置

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において、隣接して積層化される一方の上記半導体集積回路装置層はメモリセルアレーのみで構成されることを特徴する半導体集積回路装置。

【請求項１０】請求項１又は２記載の半導体集積回路装置において、積層化される複数の上記半導体集積回路装置層は主記憶装置、及び拡張記憶装置を有することを特徴とする半導体集積回路装置。

【請求項１１】請求項１又は２記載の半導体集積回路装置において、積層化される複数の上記半導体集積回路装置層は主記憶装置及びキャシュ記憶装置を有することを特徴とする半導体集積回路装置。

【請求項１２】請求項１０又は１１記載の半導体集積回路装置において、積層化される他の上記半導体集積回路装置層は中央処理装置を有することを特徴とする半導体集積回路装置。

【請求項１３】請求項１又は２記載の半導体集積回路装置において、相接する上記半導体集積回路装置層の相接する位置に対の関係で単位回路群と、その何れかを選択するスイッチとが設けられていることを特徴とする半導体集積回路装置。

【請求項１４】位置検出パターンを有する第１の基板の所望領域における位置不整を機械的または熱的外力印加により変形補正する制御手段、および位置検出パターンを有する第２の基板と該第１の基板を該位置検出パターンを用いて整合する制御手段、該第１の基板と該第２の基板を密着させる制御手段を有することを特徴とする半導体集積回路装置の製造装置。

【請求項１５】請求項１４記載の半導体集積回路装置の製造装置において、上記第１および第２の基板には半導体集積回路装置または半導体集積回路装置層が形成されていることを特徴とする半導体集積回路装置の製造装置。

【請求項１６】請求項１４または１５記載の半導体集積回路装置の製造装置において、上記第１の基板は可視光に対して透明であることを特徴とする半導体集積回路装置の製造装置。

【請求項１７】請求項１４または１５、あるいは１６記載の半導体集積回路装置の製造装置において、上記第１または該第２の基板の主表面を平面または所望曲面に保持する制御手段を有することを特徴とする半導体集積回路装置の製造装置。

【請求項１８】第１の半導体集積回路装置が構成された第１の基板の主表面を平坦化する工程、平坦化された該表面に第１の接着層を介して平坦な第２の基板とを接着する工程、該第１の基板を裏面側から所望厚さまで薄化しその表面を平坦化する工程、薄化及び平坦化した該表面に第２の接着層を介して可視光に透明な第３の基板と接着する工程、第１の接着層を除去し、第１の基板の主表面を露出する工程、第２の半導体集積回路装置が設けられ、且つ主表面が平坦化された第４の基板と該第１の

基板の主表面を整合させ、かつ接着する工程、該第２の接着層を除去し、薄化及び平坦化した該表面を露出させる工程、該第１の半導体集積回路装置の所望領域を貫通し、該第２の半導体集積回路装置の所望領域に達する開孔を設け、接続配線する工程とを有することを特徴とする半導体集積回路装置の製造方法。

【請求項１９】請求項１８記載の半導体集積回路装置の製造方法において、上記接着は断面構造を一にする半導体集積回路装置層間で行うことを特徴とする半導体集積回路装置の製造方法。

【請求項２０】請求項１８記載の半導体集積回路装置の製造方法において、上記第３の基板の所望個所に上記第２の接着層に対する溶媒の注入孔が設けられていることを特徴とする半導体集積回路装置の製造方法。

【請求項２１】請求項１８記載の半導体集積回路装置の製造方法において、開孔を介する接続工程に代えて上記第１の半導体集積回路装置層と上記第２の半導体集積回路装置層を接着面に露出された金属面で互いに接続配線することを特徴とする半導体集積回路装置の製造方法。

【請求項２２】請求項１８記載の半導体集積回路装置の製造方法において、上記第４の基板と上記第１の基板の主表面を整合させ、接着する工程を接着剤を用いず直接接着し、かつ上記第２の接着層を除去の後、接着強度を強める熱処理を施すことを特徴とする半導体集積回路装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はＳＯＩ（シリコンオンインシュレータ）基板を用いて超高集積化された半導体集積回路装置とその製造方法、並びにその製造装置に関する。

【０００２】

【従来の技術】半導体装置が形成された単結晶半導体基板の上に絶縁膜を形成し、該絶縁膜を介して非晶質半導体薄膜を堆積し、該半導体基板を結晶核としてレーザーアニール等により該半導体薄膜を単結晶化させてから該半導体薄膜に半導体装置を製造する手法が特開昭６２－２０３３５９号に開示されている。この方法により製造された半導体装置の断面図を図２７に示す。図において、第２の半導体集積回路層２０２の単結晶化が全領域で実現できれば半導体装置としての理想的な構造である積層構造半導体装置が製造できる。上記手法の長所は第１の半導体集積回路層２０１と整合させて第２の半導体集積回路層２０２への半導体装置の製造、及び第１の半導体集積回路層２０１との層間配線２０５が可能であり、構造上からは微細化に適していることである。なお、ここで２０３は絶縁層、２１１は第１層の配線層、２２１は第２層の配線層、２１２は第１層の活性領域、２２２は第２層の活性領域、２１３は第１層のゲート電極を表す。

【０００３】しかしながら非晶質膜にレーザー又は電子線照射等を施し、単結晶化する手法では単結晶化は結晶核領域の極近傍に限られ、結晶核領域から離れた絶縁膜２０３上の第２の半導体集積回路層２０２は多結晶化されるだけであり、大規模で高性能な半導体装置を該第２の半導体集積回路層２０２全面にわたり製造することは困難である。更に上記手法に於いては第２の半導体集積回路層２０２への再結晶化熱処理はもとより第２の半導体集積回路層２０２への半導体装置製造時の高温熱処理が第１の半導体集積回路層２０１にも施されることは避けられない。従って、第１の半導体集積回路層２０１内の拡散層不純物分布を急峻なまま保持することが困難となり超微細な半導体装置を第１の半導体集積回路層２０１に構成することは困難である。上記欠点はメモリセルアレーのごとく消費電力がそれほど大きくなく、かつ同一アクセス速度の素子を大容量化する目的のため積層化せんとする要求を満たす上で最大の問題点となる。積層半導体装置間でアクセス速度を同じく構成するためには素子形状はもとより同一熱処理条件の基に製造され、同一特性を有することが必要条件であるが上記従来製造方法に基づく限り第１の半導体集積回路層２０１が余分な高温熱処理工程を被ることは免れない。

【０００４】半導体薄膜の結晶性を確保するために半導体装置または半導体集積回路装置が構成された二枚の単結晶半導体基板を接着させ、一方を研磨等により薄膜化させる手法が例えばワイ．ハヤシ他、「ファブリケイションオブ　スリージメンジョナル　アイシ　ユウジング　カミュレイテブリイ　ボンデッドアイシ（キュウビック）テクノロジ」(Y.Hayashi, et al.,"Fabrication of Three-DimensionalIC Using Cumulatively Bonded IC (CUBIC) Technology" 1990 Symposium on VLSI Tech., p 95 (1990))に開示されている。この方法で製造された半導体装置の断面図を図１に示す。図１において、２は素子間分離絶縁膜、９０から９２は半導体装置と接続された電極、９４、９５は表面保護絶縁膜である。絶縁性接着剤９６および９９とその開孔９７、及び金属プール９３は第２の半導体基板１０１側に構成され、金属バンプ９８は第１の半導体基板１００側に構成されている。

【０００５】

【発明が解決しようとする課題】上記従来技術においては、第１の半導体基板１００と第２の半導体基板１０１の各々に構成されている半導体装置は金属プール９３と金属バンプ９８により電気的に接続されるが、半導体装置製造に用いる半導体基板１００又は１０１は５００μｍ以上の厚さと紫外又は可視光に対して透過できないほど厚いため開孔９７と金属バンプ９８間の位置合せはより波長が長く、半導体基板を透過可能な赤外線を用いて行われていた。従って、位置合せ精度に難点があり、数μｍ以下のパターン合せは困難であった。即ち、超高集積高密度半導体装置の積層化のごとく、１μｍ以下のパ

ターン間接続を目指すことは製品化の観点から不可能であった。

【０００６】本発明の目的は高性能で超高密度な集積回路装置を歩留り良く廉価で提供することにある。また本発明の他の目的は半導体装置製造における位置合せ精度を飛躍的に改善し、縦方向にも超高精度で大規模半導体集積回路層を積層化することのできる半導体装置の製造方法を提供することである。本発明の他の目的はＳＯＩ基板を従来の１０から１００倍の高精度で位置合せが可能な基板貼合せ装置を提供する事にある。

【０００７】

【課題を解決するための手段】上記目的は以下により達成される。第１の半導体集積回路装置が製造された第１の半導体基板を第１の接着剤を用いて別の基板と接着させる。第１の半導体基板を裏面側から研削及び研磨などで薄化させて第１の半導体集積回路装置層を形成し、これを透明石英基板に第２の接着剤を用いて接着する。この状態より第１の接着剤の溶媒で第１の接着剤のみを溶かし第１の半導体集積回路装置層を透明石英基板に転写させる。上記第１の半導体集積回路装置層を別途製造した第２の半導体集積回路装置又は半導体集積回路装置層とを厳密な位置合せを施し、第３の接着剤を用いて接着させる。上記の位置合せは第１の半導体集積回路装置層が数μｍ以下と十分に薄く構成されておれば石英基板は紫外線に対して透過率で５０％以上であり、十分に透過できるので紫外線を光源とする高精度のマスク合わせ装置を用いることができる。なお、第２の接着剤の溶媒は第３の接着剤を溶かさない性質の材料で構成すれば良い。

【０００８】薄膜化された半導体集積回路装置層を他の半導体集積回路装置又は半導体集積回路装置層と接着させるときに考慮せねばならぬことは半導体基板上への成膜の連続により膜中の真性応力や熱応力のために１０ｃｍ当たり１μｍ程度、初期のパターンから大きく歪み、半導体集積回路装置間の精密な位置合せを困難にすることである。上記のパターン歪を補正して精密な位置合せと接着を施すために、本発明においては第１の手法として位置合せを施すべき半導体集積回路装置が接着された一方または両方の基板に外力を印加し、歪みを補正する手法を用いた。また他の手法として、断面構造として同一成膜構成の半導体集積回路装置同士を接着させる手法を採用した。この場合、成膜により生じる歪量は何れの半導体集積回路装置においても同程度であり、歪による位置合せ不良は解消される。上記手法で接着させた半導体集積回路装置層同士をさらに接着させる場合もさらに接着する各々の層における断面構成を同一にして実施した。

【０００９】

【作用】本発明によれば超微細半導体集積回路装置を製造するのと同様に紫外線を光源とした高精度マスク位置合せ装置が利用できるので従来の半導体集積回路装置を製造するのと同様な高精度で半導体集積回路装置の積層化が可能となる。従って本発明手法を用いることにより従来の半導体装置の製造装置のままでさらに超高集積な半導体集積回路装置を実現することができる。ここにおいて、製造工程を分割し、良品の半導体層のみを積層して半導体集積回路装置を完成できるため、従来のごとき一貫製造にくらべて製造不良を大幅に低減することができる。すなわち、超高集積な半導体集積回路装置を廉価に提供することができる。更に積層化すべき半導体層の各々に半導体集積回路装置の構成素子を区別して構成し、積層化で一体化により完成された半導体集積回路装置とすることも可能となるため各々の半導体層を作り置き、所望時期に所望の組合せで積層化できる。従って、需要にすばやく対応することが新たに可能となる。また、相補型トランジスタへの適用のごとく、半導体層伝導型の場所的変換等の工程をも省略でき、製造工程数を低減することができる。本発明によれば同一半導体装置領域を有する半導体集積回路装置の積層化において、不良半導体装置部分が存在しても不良部分を非選択にし、別層の半導体装置部分を選択する構成にすることにより良品の半導体集積回路装置として動作させることができる。即ち、半導体集積回路装置の大面積化に伴って増大する良品歩留りの低下を積層化構成により大幅に改善することができる。その他本発明に基づけば構成素子の完全分離が可能であり、相補型トランジスタにおける寄生バイポーラ効果、即ち、ラッチアップ現象のごとき隣接素子間干渉や、α線照射に基づく誤動作等の不良をもほぼ完全に解消することができる。本発明によれば熱処理工程を同じくし、同一特性を有する複数の半導体集積回路装置を積層化により超大容量化できる。

【００１０】

【実施例】以下、本発明を実施例によりさらに詳細に説明する。説明の都合上、図面をもって説明するが、要部が拡大して示されているので注意を要する。また説明を簡略にするため、各部の材質、半導体層の導電型、および製造条件を規定して述べるが、本発明は材質、半導体層の導電型、および製造条件は実施例に限定されないことは勿論である。

【００１１】（実施例１）図２から図５は本発明による半導体集積回路装置の第１の実施例を製造工程順に示した断面図である。面方位（１００）、抵抗率５０Ωｃｍ、直径１２．５ｃｍ、ｐ導電型なる単結晶シリコン（Ｓｉ）基板１の主表面に公知の手法を用いて２００ｎｍ厚の熱酸化膜を所望箇所に選択的に形成して素子間分離絶縁膜２とした。続いて所望活性領域の基板表面に６ｎｍ厚のＳｉ熱酸化膜を形成してゲート絶縁膜３としてから所望領域のゲート絶縁膜を選択的に除去してから多結晶Ｓｉ膜とタングステン珪化膜の積層堆積膜によるゲート電極４および配線電極９を形成した。更にゲート電

極４をマスクにしてＮ型低抵抗拡散層６、７、８を形成してから電極保護絶縁膜１０を全面的に堆積した（図２）。

【００１２】図２の状態より溶融させたワックス２０を電極保護絶縁膜１０上に全面塗布し、透明石英基板３０に接着させた。続いてＳｉ基板１の裏面側から高精度研削装置により１０μｍ厚まで研削し、さらに機械的・化学的研磨を施して素子間分離絶縁膜２の裏面で規定される面までＳｉ基板１を薄化させた。上記研磨は回転円板上に設けられた研磨布にＳｉ基板を１．９ｘ１０⁴Ｐａの圧力で押しつけ、エチレンジアミン・ピロカテコールが添加された研磨液を供給しながら行ったが研磨の進行に伴って露出される素子間分離絶縁膜２の研磨速度はＳｉに比べて極めて遅く、１／１０⁴倍以下であった。従って、上記の研磨により単結晶Ｓｉ基板１は完全に平坦化され、素子間分離絶縁膜２で互いに絶縁された約１００ｎｍ厚の単結晶超薄膜Ｓｉが得られた。しかる後、研磨面に保護絶縁膜１６を形成した（図３）。

【００１３】図３の状態において、別途準備しておいた図２の状態まで製造した第２のＳｉ基板１１の主表面と前記保護絶縁膜１６とを後述の位置合せ装置を用いて正確な位置合せを行った後、フッ素系樹脂を接着層２１として貼合せた。接着層２１の厚さは約２μｍであった。しかる後、第２のＳｉ基板１１を１００℃に加熱し、ワックス２０を溶解させ、石英基板３０から剥離し、残置されたワックスをアセトンで洗浄除去した。上記のワックス除去工程はフッ素系樹脂よりなる接着層２１には何の影響も与えない（図４）。

【００１４】この状態より超薄膜Ｓｉ層１に構成された端子電極９、素子間分離絶縁膜２、接着層２１、及びＳｉ基板１１上の電極保護絶縁膜等を貫通し、Ｓｉ基板１１上の端子電極１５に到達する開孔を設けてから開孔への選択金属堆積を施すことにより接続配線１７を形成した。さらに、所望回路構成に基づいた配線１８を施して半導体集積回路装置を完成させた（図５）。

【００１５】上記製造方法に基づいて製造された半導体集積回路装置においては従来の積層型半導体集積回路装置に比べて構成される半導体層間の位置合せ精度を±０．５μｍと１０倍に向上することができた。これにより、開孔幅０．５μｍ、端子電極１５の幅として１．５μｍで層間を接続することができ、層間接続のためのパンプ及びプール形成に要していた領域を要することなく、基本回路単位を積層方向に直接構成できるまでに高集積化することができ回路設計の自由度を大幅に向上することができた。本実施例における積層方向の飛躍的位置合せ精度向上は超薄膜からなる透明な半導体集積回路装置層と透明石英が紫外線を透過できるため接着すべき下地の半導体集積回路装置と高精度で位置合せが可能となったことに基づく。

【００１６】本実施例に基づく半導体集積回路装置としてメモリセルアレーよりなる半導体集積回路装置層の積層化を実施したが、各半導体集積回路装置層は同一熱処理の製造工程で製造され、アクセス速度等の機能も各層間で異ならず実質同一の特性が得られ、同一平面上に同一容量のメモリセルアレーを構成した従来半導体集積回路装置に比べて良品率の向上と最大配線長さの短縮による動作速度の向上が達成された。

【００１７】なお、半導体集積回路装置の一般的な特性としては伝達遅延時間を用いることができる。

【００１８】（実施例２）図６から図８は本発明の第２の実施例による半導体集積回路装置を製造工程順に示した断面図である。前記実施例１に基づいて電極保護絶縁膜１０まで製造したＳｉ基板１に３μｍ厚の多結晶Ｓｉ膜２２を堆積してからその表面を平均二乗粗さが０．３ｎｍ以下になるごとく機械研磨を施し、平坦化させた。この状態から前記実施例１に従って透明石英板３０に溶融したワックス２０により接着させ、Ｓｉ基板１裏面から薄化により素子間分離絶縁膜２の裏面で規定される単結晶超薄膜Ｓｉを形成とその裏面への保護絶縁膜１２の形成を行った（図６）。

【００１９】図６の状態において、図６と同様の製法により厚い多結晶Ｓｉ膜２４の堆積とその表面の平坦化研磨まで別途製造した単結晶Ｓｉ基板１１の主表面と前記保護絶縁膜１２とを後述の位置合せ装置を用いて正確な位置合せを行った後、フッ素系樹脂を接着層２３として貼合せた。接着層２３の厚さは約０．５μｍであった（図７）。

【００２０】しかる後、第２のＳｉ基板１１を１００℃に加熱し、ワックス２０を溶解させ、石英基板３０から剥離し、残置されたワックスのアセトンによる洗浄除去と多結晶Ｓｉ膜２２の選択エッチングを施した。上記のワックス除去工程はフッ素系樹脂よりなる接着層２３には何の影響も与えない。次に単結晶超薄膜Ｓｉ層１に構成された電極配線９上において、電極配線９、接着層２３、及びＳｉ基板１１上の電極保護絶縁膜等を貫通し、Ｓｉ基板１１上の電極配線１５に到達する開孔を設けてから開孔側壁への絶縁化処理をほどこしてから開孔への金属膜の堆積とパターン形成を施すことにより接続配線１７を形成した。さらに、所望回路構成に基づいた配線１８を施して半導体集積回路装置を完成させた（図８）。

【００２１】上記製造方法に基づいて製造された半導体集積回路装置においては従来の積層型半導体集積回路装置に比べて構成される半導体層間の位置合せ精度を±０．３μｍと２０倍に向上することができた。これにより、開孔幅０．４μｍ、電極配線１５及び１７の幅として１．０μｍで層間を接続することができ、層間接続のためのパンプ及びプール形成に要していた領域を要することなく、基本回路単位を積層方向に直接構成できるまでに高集積化することができ回路設計の自由度を大幅に

向上することができた。本実施例における積層方向の飛躍的位置合せ精度向上は超薄膜からなる透明な半導体集積回路装置層と透明石英が紫外線を透過できるため接着すべき下地の半導体集積回路装置と高精度で位置合せが可能となったことに基づく。更に、前記実施例１の場合に比べてさらに位置合せ精度が向上できたのは貼合せるべき表面の凹凸を極端に平坦化したことにより接着層２３を薄く構成しても気泡の発生なしで貼合せが可能となったためと考えられる。

【００２２】（実施例３）図９から図１１は本発明の第３の実施例による半導体集積回路装置を製造工程順に示した断面図である。前記実施例２に基づいて厚い多結晶Ｓｉ膜２４表面の平坦化研磨までを施した単結晶Ｓｉ基板１をワックス２５で別途準備された鏡面Ｓｉ基板４０に貼合せた。しかる後、単結晶Ｓｉ基板１の裏面側から薄化し、素子間分離絶縁膜２裏面で膜厚が規定されるごとく前記実施例１に基づいて超薄膜単結晶Ｓｉ層を形成した（図９）。

【００２３】図９の状態まで製造した超薄膜単結晶Ｓｉ層１の裏面側に水溶性接着剤であるポリビニルアルコール膜２６を塗布し、透明石英基板３０に貼合せた。しかる後、鏡面Ｓｉ基板４０を１００℃に加熱し、ワックス２５を溶解させて石英基板３０から剥離し、残置されたワックスをアセトンにより洗浄除去した。アセトン洗浄において、ポリビニルアルコール膜２６は何等影響を受けない（図１０）。

【００２４】前記実施例２に基づいて厚い多結晶Ｓｉ膜２７表面の平坦化研磨までを施した別途準備の単結晶Ｓｉ基板１１を図１０の状態の超薄膜単結晶Ｓｉ層１と多結晶Ｓｉ面同士で直接貼合せた。上記の貼合せにおいて互いの位置合せは前記実施例２と同様に後述の精密位置合せ装置に基づいて実施した。なお、単結晶Ｓｉ基板１１には前記実施例１に基づいてＮ型低抵抗拡散層６、７、８を予め形成しておいた。上記の直接貼合せの後、単結晶Ｓｉ基板１１を水中に浸すことにより水溶性接着剤２６を溶解して透明石英基板３０から分離させ、接着強度を向上するための熱処理を９００℃、３０分の条件で施した。しかる後、単結晶超薄膜Ｓｉ層１の表面にゲート絶縁膜を形成してからゲート電極４が延在された素子間分離絶縁膜２に開孔を施した。更にゲート電極４と一致するごとく第２ゲート電極１３を単結晶超薄膜Ｓｉ層１上に形成し、第２のゲート電極１３をマスクにして低抵抗拡散層６１、６２、６３等を形成した。次に単結晶超薄膜Ｓｉ層１に構成された電極配線９上において、電極配線９、多結晶Ｓｉ層２４、２７及びＳｉ基板１１上の電極保護絶縁膜等を貫通し、Ｓｉ基板１１上の電極配線１５に到達する開孔を設けてから開孔側壁の絶縁化処理を施し、開孔への金属膜の堆積とパターン形成を施すことにより接続配線１７を形成した。さらに、所望回路構成に基づいた配線１８、および電極保護絶縁膜１０を形成して半導体集積回路装置を完成させた（図１１）。

【００２５】上記製造方法に基づいて製造された半導体集積回路装置においては従来の積層型半導体集積回路装置に比べて構成される半導体層間の位置合せ精度を±０．３μｍと２０倍に向上することができた。これにより、層間接続のためのバンプ及びプール形成に要していた領域を要することなく、基本回路単位を積層方向に直接構成できるまでに高集積化することができ回路設計の自由度を大幅に向上することができた。本実施例における積層方向の飛躍的位置合せ精度向上は超薄膜からなる透明な半導体集積回路装置層と透明石英が紫外線を透過できるため接着すべき下地の半導体集積回路装置と高精度で位置合せが可能となったことに基づく。

【００２６】さらに、本実施例に基づく半導体集積回路装置においては接着剤を用いずに直接貼合せる手法を用いているため、積層化後にゲート電極１３と拡散層６１から６３等を製造することができる。従って、積層化する半導体集積回路装置層は電流制御を超薄膜Ｓｉ層の上下から行う構成が可能となり、従来構造トランジスタ構造比で３倍以上の大電流化、即ち高速化が縦方向の超高集積化と併せて可能となった。

【００２７】（実施例４）図１２は本発明の第４の実施例による半導体集積回路装置を示した断面図である。前記実施例３において、半導体集積回路装置層１を貼合せるべき半導体基板１１の代わりに前記実施例３に記載した手法に準じて製造した超薄膜の半導体集積回路装置層１が直接貼合された半導体基板３１を用いた。半導体集積回路装置層１にはゲート電極１９や他の電極などを予め構成しておく。図９においては鏡面Ｓｉ基板４０と単結晶Ｓｉ基板１をワックス２５により接着させたが本実施例の半導体集積回路装置においては主表面に熱酸化膜２９が形成された鏡面Ｓｉ基板３１の主表面と単結晶Ｓｉ基板１上の平坦化研磨された多結晶Ｓｉ膜２８面とで接着剤なしに直接貼合せた。その後、接着強度向上のための熱処理を９００℃、３０分の条件で施してから単結晶Ｓｉ基板１の裏面側から薄化し、素子間分離絶縁膜２底面で膜厚が規定される半導体集積回路装置層１を形成した。しかる後、半導体集積回路装置層１の新規の主表面にゲート絶縁膜の形成と素子間分離絶縁膜２領域における所望個所への開孔を施してからゲート電極５を含む電極とゲート電極５と自己整合で低抵抗拡散層を形成した。続いて電極保護絶縁膜と厚い多結晶Ｓｉ膜を全面に堆積し、多結晶Ｓｉ膜の表面を平坦に研磨した。上記手法に基づいて製造した半導体基板３１上の多結晶Ｓｉ膜表面と、石英基板３０にポリビニルアルコールを接着剤２６として貼合せたゲート電極４などが構成された別途準備の超薄膜半導体集積回路装置層１（図１０）における多結晶Ｓｉ面とを接着剤無しに直接貼合せた。上記の貼合せ工程において、互いの超薄膜半導体集積回路装置

層間の位置合わせは前記実施例２または３と同様に後述する精密位置合せ装置を用いて実施した。貼合せ工程の終了後、ポリビニルアルコールによる接着剤２６の除去による透明石英板３０の分離、接着強度向上の熱処理、更には貼合せた単結晶超薄膜Ｓｉ層に第２のゲート電極１３、拡散層などの形成を前記実施例３に従って施した。この状態から主表面に露出されている単結晶超薄膜Ｓｉ層に形成されている拡散層とその底部に構成された多結晶Ｓｉ層などを貫通し、埋込まれた単結晶超薄膜Ｓｉ層上の電極に達する開孔を施した。最後に多結晶Ｓｉ側面の絶縁化処理の後、開孔への金属膜の選択形成と所望回路構成に基づく配線、及び電極保護絶縁膜を形成して半導体集積回路装置を完成させた（図１２）。

【００２８】上記製造方法に基づいて製造された半導体集積回路装置においては前記実施例３による半導体集積回路装置と同様に従来の積層型半導体集積回路装置に比べて構成される半導体層間の位置合せ精度を２０倍以上向上することができ、層間接続のためのバンプ及びプール形成に要していた領域を削減しできた。これにより基本回路単位を積層方向に構成できるまでに高集積化することが可能となり、回路設計の自由度を大幅に向上することができた。本実施例における積層方向の飛躍的位置合せ精度の向上は超薄膜からなる透明な半導体集積回路装置層と透明石英基板が紫外線をできるため接着すべき下地の半導体集積回路装置と高精度で位置合せが可能となったことに基づく。

【００２９】更に本実施例に基づく半導体集積回路装置においては積層化された何れの半導体集積回路装置層も接着剤を用いない直接貼合せによる手法に依ったため拡散層形成等、高温熱処理を要する構造を積層貼合せ工程の後に施すことか可能となった。これにより積層半導体集積回路装置層の何れの層にも半導体層の上下に電流制御のためのゲート電極を構成することが可能となり、前記実施例３の半導体集積回路装置に比べても更に高速動作が実現できた。即ち、従来構造の半導体集積回路装置に比べて積層化による超高集積化と超高速化が同時に実現できた。

【００３０】（実施例５）図１３は本発明の第５の実施例による半導体集積回路装置を示した断面図である。前記実施例４において、半導体基板３１と直接貼合せるべき超薄膜半導体集積回路装置層１の形成に関し、半導体基板３１との貼合せ面を構成する多結晶Ｓｉ膜２８の堆積に先立って接地電位を印加すべき端子部７上の電極保護絶縁膜に所望の開孔を施してから全面に低抵抗多結晶Ｓｉ膜とタングステン（Ｗ）珪化膜の第一の積層膜４２を形成した。しかる後、全面に第２の電極保護絶縁膜を堆積してから多結晶Ｓｉ膜２８の堆積とその平坦化研磨等を前記実施例４に従って施した。また、前記実施例４の製造工程においてゲート電極１３の形成の後、上部の超薄膜半導体集積回路装置層を貫通する開孔を施すにあたり、上部の超薄膜半導体集積回路装置層における接地電位を印加すべき端子部において下地の超薄膜半導体集積回路装置層を貫通し、積層膜４２に達する開孔を施し開孔部に接続用金属膜を埋め込んだ。更に前記実施例４の製造工程において、上部の超薄膜半導体集積回路装置層の主表面に電極保護絶縁膜４１を堆積した後、電源電位を印加すべき上部及び下部の超薄膜半導体集積回路装置層の所望端子部６２に開孔を施してから再び全面に低抵抗多結晶Ｓｉ膜とタングステン（Ｗ）珪化膜の第２の積層膜４３を形成した。最後に第１及び第２の積層膜、４２及び４３に対して各々接地電位及び電源電位が印加されるように所望箇所で接続させた（図１３）。

【００３１】上記製造方法に基づいて製造された半導体集積回路装置においては前記実施例４による半導体集積回路装置における積層方向への超高集積化および超高速化の特長を同様に有する。更に本実施例による半導体集積回路装置においては前記実施例４に比べてもより高速動作化が実現できた。本実施例の半導体集積回路装置ではチップ上の何れの電源電圧印加端子、及び接地電位印加端子とも半導体集積回路装置層の上下部にほぼ全領域で面状に構成された導体層に接続されている。これにより電圧供給点から各端子までの層抵抗で接地抵抗及び電源抵抗が規定され、従来半導体集積回路装置のごとく電圧供給点から各端子までの引き回された配線の実効長及び幅に基づく配線抵抗で規定される場合に比べて接地抵抗及び電源抵抗を格段に低減出来た。接地抵抗及び電源抵抗の低減効果は半導体集積回路装置の占有面積が大きくなるほど有効である。

【００３２】（実施例６）前記実施例５において、半導体基板３１と多結晶Ｓｉ膜２８を介して直接貼合せる超薄膜半導体集積回路装置層にはＮチャネル型ＭＯＳトランジスタのみを、また該超薄膜半導体集積回路装置層の上部に積層で構成する超薄膜半導体集積回路装置層にはＰチャネル型ＭＯＳトランジスタのみを構成して相補型ＭＯＳトランジスタによる半導体集積回路装置を積層構成で製造した。７は接地電位印加端子、６２は電源電位印加端子である。相補型ＭＯＳトランジスタのためのＮチャネル及びＰチャネルトランジスタの接続は超薄膜間の層間接続配線１７によった。

【００３３】上記製造方法に基づいて製造された半導体集積回路装置においてはＮチャネル型ＭＯＳトランジスタとＰチャネル型ＭＯＳトランジスタとが別々の超薄膜に構成されるので従来の相補型ＭＯＳトランジスタの構成のごとく半導体基板を各導電型のトランジスタが構成される領域（ウエル領域と称される）に分離する製造工程、およびそのための占有領域が削減されるので製造原価の低減、及び更なる高集積化が実現できた。また導電型の異るトランジスタは層を別にして完全に分離されていのでラッチアップ現象等の隣接素子間の相互干渉も完全に解消された。

【００３４】（実施例７）図１４から図１５は本発明の第７の実施例による半導体集積回路装置を製造工程順に示した断面図である。Ｐ型低抵抗Ｓｉ基板３１の主表面側から所望パターン形状の溝穴を形成し、その溝側壁に薄い絶縁膜３２を熱酸化により形成してから該溝穴を埋めるごとく不純物が添加された低抵抗の多結晶Ｓｉ膜３３を全面に堆積した。しかる後、主表面が平坦になるごとく機械的な研磨を施して多結晶Ｓｉ膜３３領域をＳｉ基板３１から分離構成した（図１４）。

【００３５】ここにおいて、別途準備したＰ導電型の単結晶Ｓｉ基板１に所望回路構成による素子間分離絶縁膜、ゲート電極４６および４７、Ｎ型低抵抗拡散層、電極保護絶縁膜等を形成してから前記実施例１に従って素子間分離絶縁膜の底面で膜厚が規定される超薄膜単結晶半導体集積回路装置層１を形成した。上記の超薄膜を前記実施例１に基づいて図１４まで製造したＳｉ基板３１と正確な位置合せの基に接着した。接着はフロン系樹脂の塗布膜を接着剤３４として実施した。しかる後、位置合せに用いた透明石英基板を除去してから所望拡散層領域の超薄膜Ｓｉ層と直下の接着剤層３４に開孔を施し、分離された多結晶Ｓｉ膜３３と所望拡散層領域を電気的に接続する電極４９を形成した。次に全面に電極保護絶縁膜を堆積してから所望拡散層領域４８との接続のための開孔とビット線を構成する配線電極１４を形成し、一容量素子と一トランジスタを基本単位とする半導体記憶装置が形成された（図１５）。

【００３６】上記の製造方法に基づいて製造された半導体集積回路装置において、容量素子が構成される半導体基板と制御トランジスタが構成される半導体基板は個別に製造された後、貼合せにより一体化されるため容量素子の製造に関して製造工程上およびレイアウト上の制約が大幅に緩和される。従って、Ｓｉ基板３１に形成する溝の深さ、及びトランジスタ底面にまで拡張できる溝面積を所望値に設定できるので十分に大きな容量値を記憶容量素子部に実現することができた。これにより、α線照射による誤動作を格段に解消することができた。

【００３７】（実施例８）図１６は本発明の第八の実施例による半導体集積回路装置を示した断面図である。本実施例では前記実施例７において、容量素子を構成するべきＳｉ基板３１の代りに熱酸化膜３６、該熱酸化膜３６上の所望回路構成に従ってパターニングされた高融点金属珪化膜３７、及び該高融点金属珪化膜上に全面的に堆積された低抵抗の多結晶Ｓｉ膜３８が主表面に構成された半導体基板３５を用いた。高融点金属珪化膜３７は所望によりパターンイングを施さず全面的に構成したままでも良い。ここにおいて容量素子のための溝形成は多結晶Ｓｉ膜３８領域に施し、その加工表面への薄い絶縁膜の形成の後、溝領域への低抵抗多結晶Ｓｉ膜３３の埋込みを施した。しかる後、半導体基板３５の主表面上の多結晶Ｓｉ膜３３、３６等を機械的研磨により平坦化してから前記実施例７に基づき平坦化面と超薄膜Ｓｉ層との接着、及びその後の製造工程を続行して半導体集積回路装置を製造した（図１６）。

【００３８】上記の製造方法に基づいて製造された半導体集積回路装置においては容量素子の一方の電極を構成する多結晶Ｓｉ膜３８は電気的に更に低抵抗な高融点金属珪化膜３７に接続され、プレート電位の印加に対し、より高速に追随できた。これにより、記憶の読出し、書込みの速度を実施例７の半導体集積回路装置に比べて更に高速化することができた。

【００３９】（実施例９）図１７は本発明の第９の実施例による半導体集積回路装置を示した断面図である。本実施例においては前記実施例２に基づいて半導体集積回路装置の積層化を繰返して多層構成の半導体集積回路装置を製造した。図１７において、１１は半導体支持基板、５０は第１の超薄膜Ｓｉ層で主記憶装置を構成した。５１、５２、５３は第２、第３及び第４の超薄膜Ｓｉ層で各々拡張記憶装置を構成した。

【００４０】本実施例に基づく半導体集積回路装置においては精密位置合せ多層構造による縦方向の高集積効果により従来半導体集積回路装置における配線遅延に基づく演算処理時間の増加を大幅に低減することができた。

【００４１】（実施例１０）本実施例においては前記実施例９の５１、５２、５３としてキャシュ記憶装置で構成した。キャシュ記憶装置の構成半導体装置は超高速バイポーラ型トランジスタによった。主記憶装置５０はＭＯＳ型トランジスタで構成した。

【００４２】本実施例に基づく半導体集積回路装置においては精密位置合せ多層構造による縦方向の高集積効果によりキャシュ記憶装置と主記憶装置間の記憶データのやりとりが瞬時に可能となるため、大容量のキャシュ記憶をそなえることができた。これにより記憶装置全体として見た場合の動作速度を大幅に向上でき、かつ大容量の情報を蓄積することが可能となった。

【００４３】（実施例１１）図１８は本発明の第１１の実施例による半導体集積回路装置を示した断面図である。本実施例においては前記実施例１０に基づいて半導体集積回路装置の積層化を繰返して多層構成の半導体集積回路装置を製造した。図１８において、５４は中央処理装置、５０は主記憶装置、５１から５３は命令プロセッサ、システム制御装置、入出力プロセッサ、拡張記憶装置等でこれらを前記実施例２に基づいて複数層にわたり積層化し、超高速計算機を構成する半導体集積回路装置とした。

【００４４】本実施例に基づく半導体集積回路装置においては精密位置合せ多層構造による縦方向の高集積効果により装置間接続長さが極端に短縮された。これにより半導体装置等の組立てによる従来大型計算機に比べて１秒間当たりの命令処理回数が大幅に増加できた。

【００４５】（実施例１２）図１９及び図２０は本発明

の第１２の実施例による半導体集積回路装置を示した断面図である。本実施例の第１の手法を図１９に、第２の手法を図２０に示す。図１９は前記実施例２と同様な製造方法に基づいて製造した本実施例の半導体集積回路装置であるが、同一機能を有する半導体集積回路装置層を上下整合させて積層構成した。更に、各半導体集積回路装置層における所望単位回路ごとにその電流経路を制御するトランジスタを直列に配置させた。５５及び５６は隣接する各半導体集積回路装置層における該トランジスタのゲート電極である。

【００４６】本実施例に基づく半導体集積回路装置においては半導体集積回路装置の大面積・大規模化に伴い低下する良品歩留りを向上させることができた。即ち、積層化された何れかの半導体集積回路装置層における所望単位回路に不良が生じていた場合、不良回路に直列接続されたトランジスタ（例えばゲート電極５５で制御されるトランジスタ）によりその経路を遮断し、接続配線電極１７を介して良品の所望単位回路側の経路のみを選択するごとくトランジスタ（例えばゲート電極５６で制御されるトランジスタ）を導通させた。これにより、従来は１箇所の不良回路の存在で半導体集積回路装置が不良とされ、良品歩留りを大幅に低下させていた状況を大幅に改善することができ、半導体集積回路装置の更なる大面積・大規模化に路を開くことができた。なお、各半導体集積回路装置層の不良箇所は各半導体集積回路装置層を形成した段階で予め測定により確認してから積層化している。

【００４７】本実施例の他の手法は図２０に示される半導体集積回路装置であり、前記実施例４に準じて同一機能を有する半導体集積回路装置層を上下整合させて積層構成した。前記実施例４との違いは各半導体集積回路装置層の製造の後、その所望単位回路の不良部分を電気測定により同定し、その不良単位回路（図２０において例えば上部半導体集積回路装置層の図示した領域）の電流経路を微細に絞ったレーザー光線により溶融により断線させ、電気的に開放状態の領域３９とした。これによりこれにより図２０の半導体集積回路装置において電流経路は接続配線電極１７を介して良品の所望単位回路側の経路（図２０において例えば下部半導体集積回路装置層の図示した領域）を選択する構成が実現できた。即ち、図１９で断面を示した本実施例の他の手法の場合と同様な不良単位回路部分の救済が可能となった。本手法においては図１９で示した半導体集積回路装置に比べて不良単位回路救済に要する余分のトランジスタを必要とせず、従って、占有面積の増大を防止でき、半導体集積回路装置の大面積・大規模化を更に推し進めることが可能となった。

【００４８】（実施例１３）図２１と図２２は本発明の半導体集積回路装置の製造装置を示す概念図である。前記各実施例の半導体集積回路装置は本実施例の製造装置を用いて製造された。パターンが形成された２枚の半導体基板又は半導体薄膜７５および７６を高精度で位置合せし、互いに接着するためには成膜に基づく各々の半導体基板又は半導体薄膜独自の伸縮及び歪等を互いに精度良く整合するべく矯正する必要がある。図２１において、第１のステージ７１上に第２のステージ７２及び第３のステージ７３を配置している。ステージ７２上に基板７５を、ステージ７３上には基板７６を真空吸着した。それぞれの基板はステージに相対的にプレアライメントされた状態でステージ上に搬送される。基板の搬送は通常方式の自動搬送機構を用いた。ステージ７２およびステージ７３はそれぞれ回転機構を有しており、ステージの移動軸に基板上のチップ配列が平行になるように合わせることができる。基板上には位置認識用のターゲットマークが形成されており、ターゲットマークの位置検出は位置検出光学系７７、７８で行う。この装置では基板７５に対して基板７６を整合する構成となっている。検出光学系７７、７８で基板７５及び基板７６の相対位置誤差を測定し、位置誤差が存在する場合、ステージ７３上の基板変形機構により基板７６を変形させ、基板７５と相対的な位置誤差が無くなるように制御する。ステージ７３上には細分化された基板吸着ブロックが配置されており、それぞれのブロック７４はピエゾ素子により単独で移動ができるように構成されている。基板の位置はステージマーク８０及び８１に対し相対的に認識される。基板７５と基板７６はミラー反転した位置関係となっており、双方の位置関係は位置認識部７９からの情報に基づいてコンピュータ制御系８３でデータ処理される。そのデータを基板変形制御機構８２で処理し、細分化された基板吸着ブロック７４を移動させ、基板７６を変形させる。この動作により基板７５に対して基板７６がミラー反転した状態で同一形状にすることができる。

【００４９】次のステップでは図２２に示すように基板７５をステージ７２に固定した状態で鏡面反転し、基板７６の主表面と基板７５の主表面が対向するように移動する。移動機構は図示していないが通常のアーム式移動機構を用いた。この状態でステージマーク８０及び８１を位置検出光学系８４を用いて位置検出する。このデータはコンピュータ制御系８３でデータ処理される。このデータをステージ位置制御系８５で処理し、ステージ７３を移動機構８６で移動し、ステージ７２に相対的に位置決めする。その後、ステージ７２の上下移動機構により基板７２を下降させ、基板７３と密着させることにより貼合せが完了する。貼合せを良好に行うため、ステージ７２は僅かな傾きが設定できるようになっている。上記一連の動作により互いに異なった変形を有する基板７５及び基板７６を同一形状に矯正して貼合せることができる。上記実施例において、基板７６の変形機構には細分化した基板吸着ブロック７４をピエゾ素子により移動

する機構を用いたが他の手法に基づいてもよい。例えば吸着ブロック７４を熱変形板で移動する方式や、液体や気体の圧力を利用して位置を変える方式など種々可能である。即ち、本装置の特長は基板の形状を自在に変形できる機構を有することにある。なおここでは本装置の機能を説明するため装置を細分化して説明したが図２１及び図２２は同一装置内でも別装置で構成されていても本実施例による製造装置の特徴は変わらない。また、本実施例による製造装置の特徴に直接関係しない機構については説明を省略したが、通常の位置整合装置で必要な機構は付加されている。例えば装置全体の温度制御機構、ステージ位置測長機構、基板カセット・ツウ・カセット搬送機構等がその例である。また、本装置の変形として図２２のように基板７５の裏面からチップ配列の変形を測定することも可能である。基板７６の変形を測定する場合はステージ７２を検出の邪魔にならない位置に退避させる必要がある。この場合、図２１のステージ７１は不要となり、装置の小型化が達成できる。本実施例の製造装置を用いる基板７５または７６としては半導体集積回路装置が製造された通常の単結晶半導体基板に限定される必要はなく、前記実施例１等に記載したごとき支持基板としての半導体基板上に接着剤で貼合せた単結晶超薄膜Ｓｉ膜に製造された半導体集積回路装置層であってもよい。上記単結晶超薄膜Ｓｉ膜は接着剤を用いない直接貼合せによるものであってもよい。この場合、本実施例に基づいた厳密な位置合せと密着および接着が半導体集積回路装置層間で施された後、本実施例の製造装置から基板７５および７６をはずしてから接着剤の溶媒中に該基板を浸して、支持基板を外せばよい。接着剤を用いない直接貼合せの場合は支持基板を研削・研磨等で除去する。

【００５０】（実施例１４）前記実施例１３においては図２１に示すごとく、基板７５及び７６上の位置認識ターゲットを用いた位置検出を各基板７５及び７６の主表面を上にした状態で行った。本実施例では基板７５及び第２のステージ７２を可視光、更には紫外光を透過できる構成にすることにより基板７５をミラー反転した状態、即ち図２２に示すごとく基板７５及び７６がそのままできる状態で施した。第２のステージ７２は省略し、基板７５と基板７６上の位置認識用ターゲットマーク間で識別してもよい。ここにおいて、基板７６上の位置認識用ターゲットマークは検出光学系７７により基板７５を透過して識別される。本実施例によれば前記実施例１３で用いたステージマーク８０及び８１による基板間の位置合せ機構が省略でき、基板７５及び７６間のより直接的な位置合せが可能となって装置の簡略化が実現できた。更に前記実施例１３においては基板７５と第２のステージ７２と間で大幅な位置不整合が存在した場合、位置認識が不可能となる欠点が生じるが、本実施例においては基板７５及び７６間の大幅な位置不整合の存在は一目瞭然であり、簡単に修正できる。

【００５１】本実施例において、基板７５及び第２のステージ７２を紫外光が透過する構成にすることにより通常のＳｉ基板のごとく赤外光しか透過できない場合に比べて、より短波長の検出光学系７７が使用可能となる。従って、より精密な位置検出が可能となる。紫外光に対する透過特性と容易に入手できることを考慮すると第２のステージ７２は透明石英基板であることが望ましく、基板７５は該透明石英基板に（特に紫外光も透過可能なフロン樹脂系の）薄い接着剤により貼合された単結晶Ｓｉ超薄膜の半導体集積回路装置層であることが望ましい。ここにおいて、Ｓｉ超薄膜の膜厚は紫外光透過の条件から１００ｎｍ以下であることが望ましい。本実施例により精密な位置検出とその後の接着、及び超薄膜化等の工程を施された基板７５及び７６は前記実施例１又は２に基づいて該透明石英基板を除去し、超薄膜が形成される。

【００５２】前記実施例１３、及び１４において、基板７５及び７６間の精密な位置合せを阻害する要因は基板７５及び７６の各々に構成する集積回路装置の製造に不可欠の基板上成膜に基づく。即ち、基板上に形成する各種絶縁膜や金属膜自身が有する内部応力や基板上成膜の状態で施される各種熱処理により基板との熱膨張係数の違いに基づき熱応力により半導体集積回路装置又は半導体集積回路装置層か構成された基板は上に凸又は凹になるごとく反りを生じ、基板表面のパターンに歪み及び伸縮をもたらす。上記のパターン歪み及び伸縮は基板周辺領域において特に顕著となる。２枚の基板間の精密な位置合せを行う段階において上記パターン歪み及び伸縮の影響を大幅に緩和するには集積回路装置が製造された２枚の基板の反りを同一に制御すれば解決できる。その一手法として、２枚の基板が各々平面になるごとく構成する。具体的には前記実施例１３、及び１４において、ステージ７２上に基板７５を、ステージ７３上には基板７６を真空吸着したが、該真空吸着を表面が極めて平坦で多数の吸引孔を有するステージにより該基板を強く吸着することで実現できる。吸引孔の数を多く構成するほど吸着基板はステージの形状に一致することができ、多孔構成によるステージが望ましい。これにより精密な位置合せを行う２枚の基板の主表面を平坦に保持し、パターン歪み及び伸縮を最小限に抑えることが可能となる。２枚の基板の主表面におけるパターン歪み及び伸縮を同一に制御する観点から該主表面は必ずしも平面である必要はなく、パターン歪み及び伸縮が同一になるごとく所望曲面に制御してもよい。

【００５３】（実施例１５）図２３は本発明の第１５の実施例による半導体集積回路装置の製造方法を示す断面図である。本実施例においては２枚の基板間位置合せを更に厳密ならしめる手法を追及した。前述したごとく、基板表面に形成されたパターンの伸縮及び歪は集積回路

装置の製造過程で基板上に形成する各種絶縁膜及び金属膜の膜厚と各種膜の形成後における熱処理履歴に大きく依存する。従って、半導体基板上に形成された集積回路装置のパターンに集積回路装置固有の伸縮及び歪が発生することは謂ば不可避である。本実施例では上記状況を踏まえた上で正確な位置合せを保証しつつ２枚の基板を貼合せた。即ち、貼合せるべき２枚の基板はその成膜条件等の前歴が同一のものどうしで実施させた。図２３において、５７と５８は各々単結晶Ｓｉ超薄膜の半導体集積回路装置層であり、前記実施例２又は３に基づいて超薄膜化とその貼合せを施した。３０は透明石英基板であり、水溶性接着剤２６及びフロン系接着剤３４により超薄膜５７と接着した。５７と５８は各々製造工程が異なり、従って超薄膜化前の段階、即ち半導体基板主表面上に半導体集積回路装置が形成された段階において半導体基板の反り量は各々異なっていた。かかる半導体基板に関し、本実施例においては線膨張係数が半導体基板と異なる絶縁膜を堆積して２枚の半導体基板の反りの方向及び量が等しくなるごとく制御した。上記絶縁膜の堆積は半導体基板の何れの面であってもよい。しかる後、前記実施例１３に記載の装置を用いて２枚の半導体基板の精密な位置合せとその接着を行った。反りの方向及び量が等しい２枚の基板間においてはパターンの伸縮及び歪量がほぼ等量となり相対的なパターン位置ズレは解消され、良好な位置合せが実施できた。

【００５４】全く同一の製造工程により製造された２組の超薄膜５７及び５８を各々透明石英基板３０に接着させ、再び前記実施例１３に記載の装置を用いてこれらを接着剤をもちず直接貼合せ、四層構造の超薄膜とした。しかる後、水溶性接着剤２６を溶融して一方の透明石英基板３０を除去してから別途準備した支持基板と接着させ、接着剤３４の溶融により他方の透明石英基板３０も除去して半導体集積回路装置を完成させた。上記四層構造の超薄膜の製造において、２組の重合せ超薄膜５７及び５８は何れも全く同一の製造工程により製造され、同一の断面構成を有している。これにより、重合せ超薄膜５７及び５８に生ずるパターン位置ズレは相対的に等しくなり、正確な位置合せが特別な対策無しに容易に実現できた。

（実施例１６）図２４は本発明の第１６の実施例による半導体集積回路装置の製造方法を示した平面図である。前述の各実施例において、本発明の半導体集積回路装置につきその製造方法を含めて説明したが何れの実施例においても半導体集積回路装置又は半導体集積回路装置層を別途準備した半導体基板、又は石英基板等に一度接着し、超薄膜化など所望の製造工程を施した後、該超薄膜を何らかの手法により他の基板と再び貼合せる手法を用いている。上記手法において、最初に接着した半導体基板、又は石英基板等を半導体集積回路装置又は半導体集積回路装置層から剥離させるが接着剤によってはその溶媒による剥離が容易でないことがある。これは接着剤厚さが薄いため溶媒が接着面に速やかに浸透しないためである。溶媒を接着面に速やかに浸透させ、石英基板７２を半導体集積回路装置又は半導体集積回路装置層７５から速やかに剥離させるため、本実施例においては剥離させるべき石英基板７２の所望箇所に図２４に示すごとく石英基板７２の裏面から表面に達する微細な貫通孔５９を複数形成したものを使用した。接着剤の種類に応じて貫通孔５９は一つであってもよい。

【００５５】前記実施例１及び２等に従った半導体集積回路装置の製造方法において、半導体集積回路装置又は半導体集積回路装置層が形成された半導体基板を石英基板に接着し、超薄膜化など所望の製造工程を施した後、別途準備した他の半導体集積回路装置又は半導体集積回路装置層と精密に位置合せを施して接着している。しかる後、該石英基板を剥離させるがこの剥離工程において本実施例に基づく石英基板７２と貫通孔５９を有しない石英基板３０についてその剥離に要する時間を比較した。溶融すべき接着剤としてポリビニルアルコール等の水溶性接着剤、及びフロン系接着剤、石英基板７２に設ける貫通孔５９の直径は１０μｍから２００μｍまで、貫通孔５９の数も１から５０個まで各種検討した。何れの場合も貫通孔５９を有する本実施例による石英基板７２を用いた方が剥離に要する時間を十分の一以下と大幅に短縮することができた。上記記載条件の貫通孔５８を有する石英基板７２は予め接着する工程、及びその後の超薄膜化など所望の製造工程を通じ、貫通孔５９を有しない石英基板の場合と全く同様に作用でき、何等問題は生じなかった。

【００５６】なお、前述した各実施例において、説明を簡便化するために接着剤の材料を特定して述べたが本発明の精神は第一の接着剤の溶融に対して第二の接着剤が溶融されない性質のものであればよく、従って、その範囲内であれば接着剤の材料は何ら限定されない。また、接着剤の溶融は製造した超薄膜を他の支持基板に転写可能にするための工程であり、被接着基板の消耗による製造価格の上昇を考慮しないならば超薄膜を別の支持基板に転写した後、被接着基板を機械的研磨・研削により除去してもよい。

【００５７】（実施例１７）図２５から図２６は本発明の第１６の実施例による半導体集積回路装置を製造工程順に示した断面図である。実施例２に於いて、図６の状態から保護絶縁膜１２に開口を施し、開口にＡｌを主材料とする金属膜６５及び６６を埋め込み、保護絶縁膜１２面と同一面になるごとく平坦化及び清浄化させた。更に、図６と同様の製法により別の単結晶Ｓｉ基板１１上に形成した半導体集積回路装置に厚い多結晶Ｓｉ膜２４の堆積とその表面の平坦化研磨まで行い、その表面にフッ素系樹脂による接着層２３の形成、及び半導体集積回路装置に達する開口を接着層２３に施し、開口側壁の絶

縁化処理の後、開口部にＡｌを主材料とする金属膜６７及び６８を埋め込み、接着層２３面と同一面になるごとく平坦化及び清浄化させた。しかる後、前述の位置合せ装置を用いて正確な位置合せを行って両者を接着させた（図２５）。

【００５８】しかる後、第２のＳｉ基板１１を１００℃に加熱し、ワックス２０を溶解させ、石英基板３０から剥離し、残置されたワックスのアセトンによる洗浄除去と多結晶Ｓｉ膜２２の選択エッチングを施した。上記ワックス除去工程はフッ素系樹脂よりなる接着層２３には何の影響も与えない。次に単結晶超薄膜Ｓｉ層１上において所望の回路構成に基づいて配線１８を施し、半導体集積回路装置を完成させた（図２６）。

【００５９】本実施例に基づく半導体集積回路装置としてメモリセルアレーを積層集積化したが各層のメモリセルアレーは同一製造工程、同一熱処理工程に基づいて形成され、従って同一機能を有していたが、積層集積化によっても何ら機能に変化は生じなかった。従来平面構成集積化構造における最大配線長が本実施例に基づく積層化により短縮され、アクセス速度の向上が達成できた。更に、本実施例は接着面に接続配線を露出し、露出面で接続配線ができる構成であるため本実施例手法を拡張することにより３層以上の積層化にも容易に適用できる利点を有することが明らかである。

【００６０】

【発明の効果】本発明によれば半導体集積回路装置を縦方向にも極めて精度よく整合して積層化できるので面積の増大化と無関係に半導体集積回路装置の更なる高集積化が実現できる。上記積層化に於いて、各層の半導体集積回路装置を熱処理工程を含めて全く同一特性、同一機能を保ったままで積層化が可能である。本発明によれば半導体基板の大口径化等新たな設備投資を要することなく現有半導体製造装置で次世代、次々世代に要求させる超高性能、大容量半導体集積回路装置を製造することができる。更に、本発明によればシステムを構成する種々の半導体集積回路装置を予め複数枚途中製造しておき、需要状況に応じて顧客が要望するシステムを迅速に製造し、出荷することができる。従って、製造工程の短縮とコストの低減効果がある。

【００６１】本発明によれば半導体集積回路装置を構成する基本回路を更に所望構成素子群ごとに同一の半導体基板に製造し、その積層化により一基本回路に一体化して集積回路装置とすることができる。従って、同一基板内で領域を分けて異種導電型素子を構成した従来構造に比べて領域分離に要する製造工程、及び占有面積を省略できる。また、隣接素子間の相互干渉や隣接素子製造工程に基づく素子構造の自由度の制限なども解消できる。これにより製造工程の短縮とコストの低減効果が新たに生じる。

【００６２】半導体集積回路装置の大容量化・大面積化に伴い、素子または構成回路が製造不良に陥る確率が増大するが更に本発明によれば不良領域を素子単位、又は所望単位ごとに選択し、その電流経路を正常な素子または構成回路側の領域に切替えることができる。これにより、大容量化・大面積化の半導体集積回路装置の良品歩留りを大幅に向上することができる。

【００６３】本発明によれば超薄膜の製造工程において、超薄膜を接着した第１の支持基板から他の支持基板に超薄膜を転写するにあたり該第１の支持基板を消耗することなく剥離させるので大規模半導体集積回路装置を廉価に製造することができる。

【図面の簡単な説明】

【図１】従来の半導体集積回路装置の一例を示す断面図。

【図２】本発明の実施例１の半導体集積回路装置の製造工程を示す断面図。

【図３】本発明の実施例１の半導体集積回路装置の製造工程を示す断面図。

【図４】本発明の実施例１の半導体集積回路装置の製造工程を示す断面図。

【図５】本発明の実施例１の半導体集積回路装置の完成断面図。

【図６】本発明の実施例２の半導体集積回路装置の製造工程を示す断面図。

【図７】本発明の実施例２の半導体集積回路装置の製造工程を示す断面図。

【図８】本発明の実施例２の半導体集積回路装置の完成断面図。

【図９】本発明の実施例３の半導体集積回路装置の製造工程を示す断面図。

【図１０】本発明の実施例３の半導体集積回路装置の製造工程を示す断面図。

【図１１】本発明の実施例３の半導体集積回路装置の完成断面図。

【図１２】本発明の実施例４の半導体集積回路装置の完成断面図。

【図１３】本発明の実施例５及び６の半導体集積回路装置の完成断面図。

【図１４】本発明の実施例７の半導体集積回路装置の製造工程を示す断面図。

【図１５】本発明の実施例７の半導体集積回路装置の完成断面図。

【図１６】本発明の実施例８の半導体集積回路装置の完成断面図。

【図１７】本発明の実施例９及び１０の半導体集積回路装置の完成断面図。

【図１８】本発明の実施例１１の半導体集積回路装置の完成断面図。

【図１９】本発明の実施例１２の半導体集積回路装置の製造工程を示す断面図。

【図２０】本発明の実施例１２の半導体集積回路装置の完成断面図。

【図２１】本発明の実施例１３の半導体集積回路装置の製造装置を示す概念図。

【図２２】本発明の実施例１３の半導体集積回路装置の製造装置を示す概念図。

【図２３】本発明の実施例１５の半導体集積回路装置の製造工程を示す断面図。

【図２４】本発明の実施例１６の半導体集積回路装置を示す平面図。

【図２５】本発明の実施例１７の半導体集積回路装置の製造工程を示す断面図。

【図２６】本発明の実施例１７の半導体集積回路装置を示す平面図。

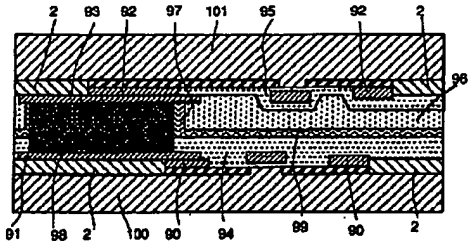
【図２７】従来の半導体集積回路装置の一例を示す断面図。

【符号の説明】

１…半導体基板、２…素子間分離絶縁膜、３…ゲート絶縁膜、４、５…ゲート電極、６、７、８…拡散層、９、１５…端子電極、１０…電極保護絶縁膜、１１…半導体基板、１４…配線、１６…保護絶縁膜、１７…接続配線、１８…配線、１９…ゲート電極、２０、２５…ワックス、２１、２３…接着層、２２、２４、２７、２８…多結晶Ｓｉ膜、２６、２９…接着層、３０…透明石英基板、３１、３５、４０…Ｓｉ基板、３２…薄い絶縁膜、３３…低抵抗多結晶Ｓｉ膜、３６…熱酸化膜、３７…低抵抗導電配線、３８…多結晶Ｓｉ膜、３９…電気的開放領域、４１、４４…電極保護絶縁膜、４２、４３…低抵抗導電膜、４５…接着層、４６、４７…ゲート電極、４９…電極、５０…主記憶装置が構成された超薄膜Ｓｉ層、５１、５２、５３…拡張記憶装置が構成された超薄膜Ｓｉ層、５４…中央処理装置が構成された超薄膜Ｓｉ層、５５、５６…電流経路制御用トランジスタのゲート電極、５７、５８…超薄膜半導体集積回路装置、５９…貫通孔、６１、６２、６３…拡散層、７１、７２、７３…ステージ、７４…ブロック、７５、７６…基板、７７、７８、８４…位置検出光学系、７９…位置認識部、８０、８１…ステージマーク、８２…基板変形制御機構、８３…コンピュータ制御制御系、８５…ステージ位置制御系、８６…移動機構、２０１…第１の半導体集積回路層、２０２…第２の半導体集積回路層、２０３…絶縁膜、２０５…層間配線、２１１…第１の配線層、２２１…第２の配線層、２１２…第１の活性領域、２２２…第２の活性領域、２１３…第１層のゲート電極。

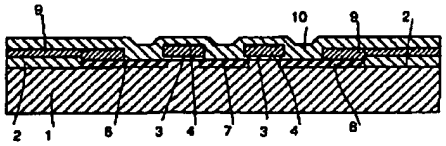
【図１】

図１



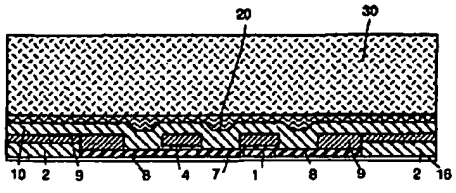
【図２】

図２



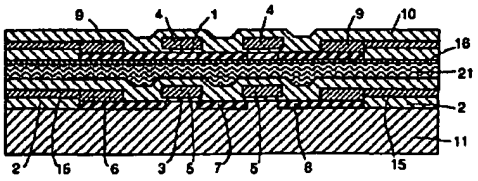
【図３】

図３



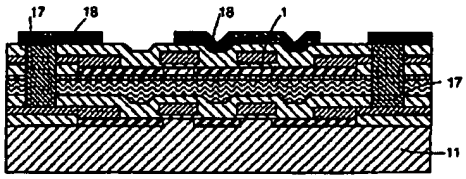
【図４】

図４



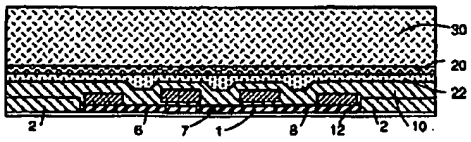
【図５】

図5



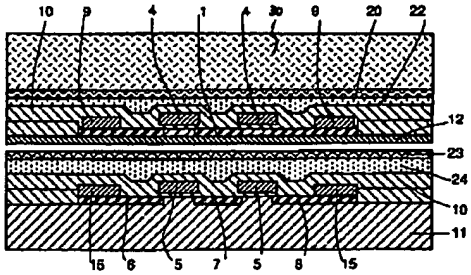
【図６】

図6



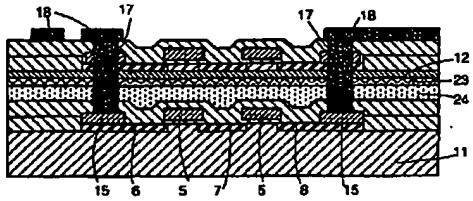
【図７】

図7



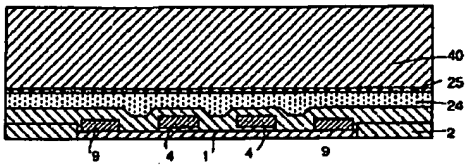
【図８】

図8



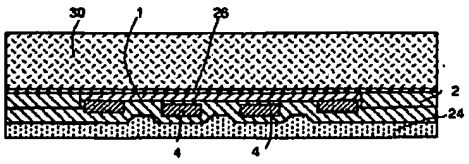
【図９】

図9



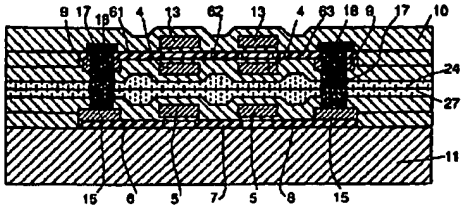
【図１０】

図10



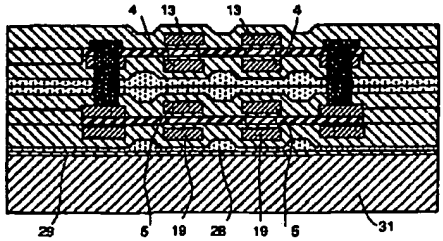
【図１１】

図11



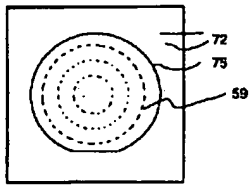
【図１２】

図12



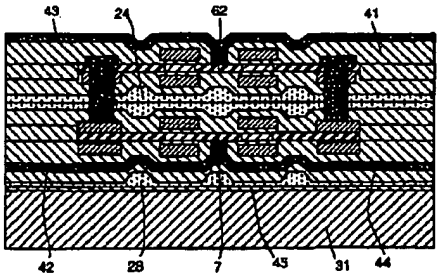
【図２４】

図24



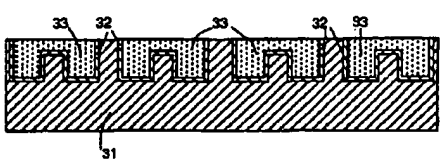
【図１３】

図13



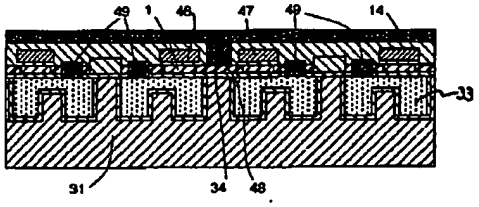
【図１４】

図14



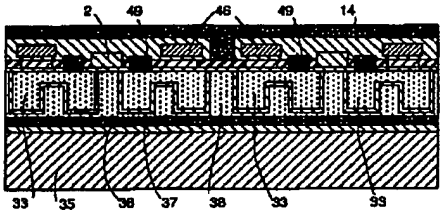
【図１５】

図15



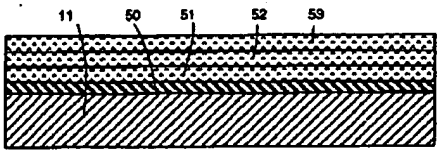
【図１６】

図16



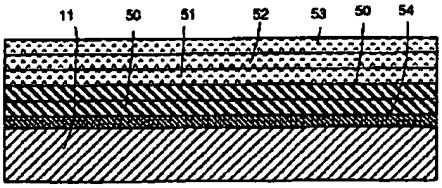
【図１７】

図17



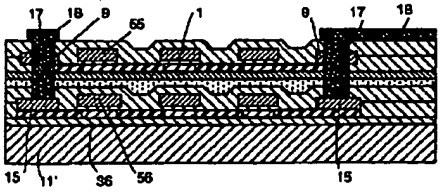
【図１８】

図18



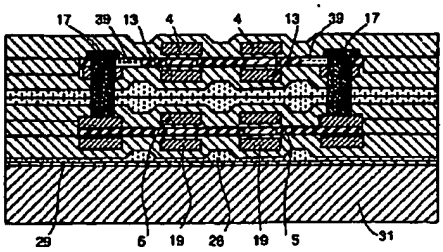
【図１９】

図19



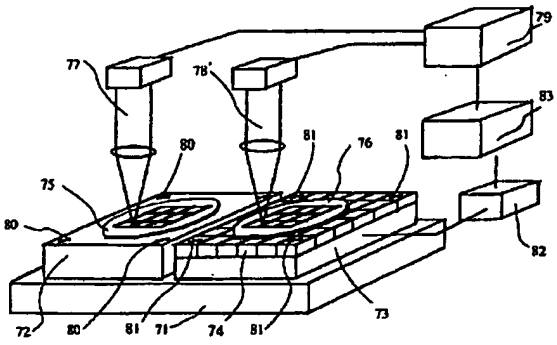
【図２０】

図20



【図２１】

図21



【図２２】

図22

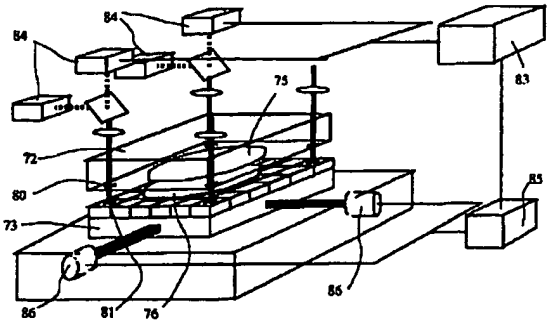


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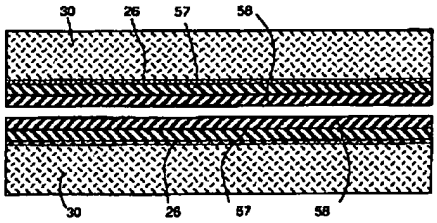
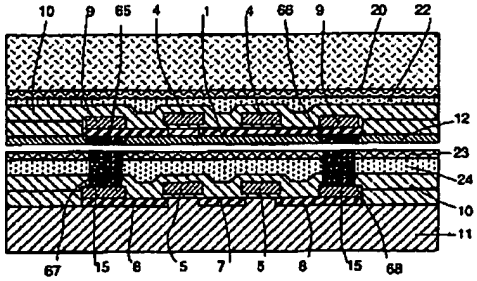
図23



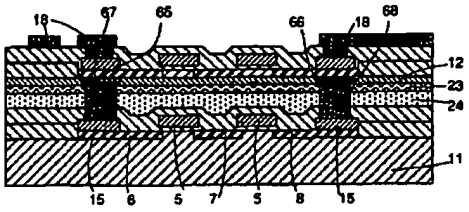
【図２５】

図25



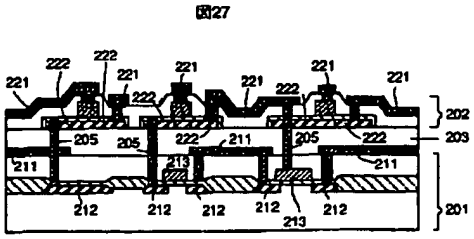
【図２６】

図26



【図２７】

図27



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Semiconductor Integrated Circuit Device and Manufacturing Method

(57) [Abstract]
[Purpose] To manufacture a high-performance and high-density large scale integrated circuit device with excellent yield by accurately aligning and laminating semiconductor layers whereupon a plurality of semiconductor integrated circuits are formed.
[Constitution] A semiconductor integrated circuit device layer is formed by laminating

a flat quartz substrate 30, which transmits ultraviolet rays, on the major surface of the semiconductor integrated circuit device formed on a semiconductor substrate with adhesive 20, and by thinning the layer. The thin layer and a separately prepared semiconductor substrate 11 mounted with a semiconductor integrated circuit device are aligned with high-accuracy by using ultraviolet rays and laminated. An aligning device provided with a mechanism which corrects pattern distortion caused in the film forming process or the like, in the whole area of the semiconductor substrate, so as to allow correct aligning is used. After the second lamination, the first adhesive is melted so as to release the quartz substrate and a laminated semiconductor integrated circuit device is formed.

[Scope of Claims]

[Claim 1] A semiconductor integrated circuit device wherein each of a plurality of single crystal semiconductor thin film regions separated from each other by an insulating film is provided with at least one semiconductor device and the semiconductor devices are connected with each other by a wiring layer so as to form semiconductor integrated circuit device layers which are laminated to structure the semiconductor integrated circuit device, comprising:

a part of semiconductor devices formed in the semiconductor integrated circuit device layer respectively, having substantially the same transfer delay time characteristics;

semiconductor device electrode terminals which are aligned to each other between the adjacent semiconductor integrated circuit device layers; and

a connecting conductor which penetrates through the terminal and reaches the terminal underneath.

[Claim 2] A semiconductor integrated circuit device wherein each of a plurality of single crystal semiconductor thin film regions separated from each other by an insulating film is provided with at least one semiconductor device and the semiconductor devices are connected with each other by a wiring layer so as to form semiconductor integrated circuit device layers which are laminated to structure the semiconductor integrated circuit device, comprising:

a part of semiconductor devices formed in the semiconductor integrated circuit device layer respectively, having substantially the same transfer delay time characteristics; and

a connecting conductor which penetrates through the single crystal semiconductor thin film region in an upper layer and is connected with the single crystal semiconductor thin film region or a wiring region in an under layer.

[Claim 3] A semiconductor integrated circuit device according to claim 1 or 2, wherein the semiconductor integrated circuit device layers having contact with each other are laminated by direct lamination without an adhesive layer therebetween.

[Claim 4] A semiconductor integrated circuit device according to claim 1 or 2, wherein the semiconductor integrated circuit device layer has wiring layers on the upper surface and the under surface both.

[Claim 5] A semiconductor integrated circuit device according to claim 4, wherein at least one layer of the wiring layers has the form of a sheet, and comprises a terminal to apply a power supply potential or a ground potential.

[Claim 6] A semiconductor integrated circuit device according to claim 1 or 2, wherein one of the semiconductor integrated circuit device layers having contact with each other is provided with a first conductivity type semiconductor device and the other is provided with a second conductivity type semiconductor device, so that they make a pair.

[Claim 7] A semiconductor integrated circuit device according to claim 1 or 2, wherein a desired region in one of the semiconductor integrated circuit device layers having contact with each other is provided with a transistor and a desired region in the other semiconductor integrated circuit device layer is provided with a capacitance element aligned with the transistor, so that they make a pair.

[Claim 8] A semiconductor integrated circuit device according to claim 7, wherein one of electrodes of the capacitance element is connected with a refractory metal film or a refractory metal silicide film, and the refractory metal film or the refractory metal silicide film is provided in the under side of the transistor.

[Claim 9] A semiconductor integrated circuit device according to claim 1 or 2, wherein one of the adjacent semiconductor integrated circuit device layers laminated is structured only by a memory cell array.

[Claim 10] A semiconductor integrated circuit device according to claim 1 or 2, wherein the plurality of semiconductor integrated circuit device layers laminated have a main storage and an extended storage.

[Claim 11] A semiconductor integrated circuit device according to claim 1 or 2, wherein the plurality of semiconductor integrated circuit device layers laminated have a main storage and a cache storage.

[Claim 12] A semiconductor integrated circuit device according to claim 11 or 12, wherein the other semiconductor integrated circuit device layer laminated has a central processor.

[Claim 13] A semiconductor integrated circuit device according to claim 1 or 2,

wherein a group of unit circuits and a switch to select any of these are provided, making a pair, in a position where the semiconductor integrated circuit device layers have contact with each other.

[Claim 14] Manufacturing equipment of a semiconductor integrated circuit device, comprising:

a control means which deforms and corrects position misalignment in a desired region in a first substrate having a position detecting pattern, by applying a mechanical or thermal external pressure;

a control means which aligns a second substrate having a position detecting pattern and the first substrate, using the position detecting pattern; and

a control means which makes the first substrate and the second substrate to stick together.

[Claim 15] Manufacturing equipment of a semiconductor integrated circuit device according to claim 14, wherein a semiconductor integrated circuit device or a semiconductor integrated circuit device layer is formed on the first and the second substrates.

[Claim 16] Manufacturing equipment of a semiconductor integrated circuit device according to claim 14 or 15, wherein the first substrate is transparent with respect to visible light.

[Claim 17] Manufacturing equipment of a semiconductor integrated circuit device according to any one of claim 14, 15 and 16, comprising a control means which maintains a major surface of the first or the second substrate as a flat surface or a desired curved surface.

[Claim 18] A method for manufacturing a semiconductor integrated circuit device, comprising the steps of:

planarizing a major surface of a first substrate where a first semiconductor integrated circuit device is structured;

bonding a second substrate which is flat to the planarized surface with a first adhesion layer therebetween;

thinning the first substrate up to desired thickness from the rear surface side and planarizing the surface;

bonding a third substrate which is transparent with respect to visible light to the surface which is thinned and planarized, with a second adhesion layer therebetween;

removing the first adhesion layer and exposing the major surface of the first substrate;

aligning and bonding the major surfaces of a fourth substrate, where a second

semiconductor integrated circuit device is provided and whose major surface is planarized, and the first substrate;

removing the second adhesion layer and exposing the surface which is thinned and planarized; and

forming a hole which penetrates through a desired region in the first semiconductor integrated circuit device and reaches a desired region in the second semiconductor integrated circuit device, and making a connection wiring.

[Claim 19] A method for manufacturing a semiconductor integrated circuit device according to claim 18, wherein the bonding is performed between semiconductor integrated circuit device layers having the same cross section structure.

[Claim 20] A method for manufacturing a semiconductor integrated circuit device according to claim 18, wherein an injected hole for a solvent for the second adhesion layer is provided in a desired part of the third substrate.

[Claim 21] A method for manufacturing a semiconductor integrated circuit device according to claim 18, wherein a connection wiring is made with exposed metal surfaces on the first semiconductor integrated circuit device layer and the second semiconductor integrated circuit device layer, instead of the step of connecting through a hole.

[Claim 22] A method for manufacturing a semiconductor integrated circuit device according to claim 18, wherein:

the major surfaces of the fourth substrate and the first substrate are aligned and bonded directly, without using an adhesive, in the step of bonding; and

a heat treatment is performed to improve adhesive strength, after the second adhesion layer is removed.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application] The present invention relates to a semiconductor integrated circuit device which is ultra-highly integrated using SOI (silicon on insulator) substrate, its manufacturing method and the manufacturing equipment for it.

[0002]

[Prior Art] A technique in which an insulating film is formed on a single crystal semiconductor substrate where a semiconductor device is formed, an amorphous semiconductor thin film is deposited with the insulating film therebetween, and a semiconductor device is manufactured on the semiconductor thin film after the semiconductor thin film is single-crystallized by laser annealing or the like with the semiconductor substrate as a crystal nucleus is disclosed in Japanese Patent Laid-Open

Publication No. 62-203359. A cross-sectional view of a semiconductor device manufactured by this method is shown in Fig. 27. In the figure, when single-crystallization of a second semiconductor integrated circuit layer 202 is realized in the whole region, a laminated structure semiconductor device with an ideal structure as a semiconductor device can be manufactured. The merit of the above-described technique is that manufacturing of a semiconductor device on the second semiconductor integrated circuit layer 202 and an interlayer wiring 205 with a first semiconductor integrated circuit layer 201 are possible, by aligning with the first semiconductor integrated circuit layer 201, so it is suitable for miniaturization structurally. Here, the numeral 203 is an insulating layer, 211 is a wiring layer of a first layer, 221 is a wiring layer of a second layer, 212 is an active region of the first layer, 222 is an active region of the second layer, and 213 is a gate electrode of the first layer.

[0003] However, with the technique in which laser, or electron irradiation or the like is applied to an amorphous film so as to single-crystallize it, the single-crystallization is limited to the very close part to the crystal nucleus region, and the second semiconductor integrated circuit layer 202 on the insulating film 203, which is far from the crystal nucleus region, is only polycrystallized. Therefore, it is difficult to manufacture a large-scale and high-performance semiconductor device on the whole surface of the second semiconductor integrated circuit layer 202. In addition, with the above-described technique, it cannot be avoided that a high temperature heat treatment to the second semiconductor integrated circuit layer 202, performed when manufacturing a semiconductor device, as well as a recrystallization heat treatment to the second semiconductor integrated circuit layer 202, is also applied to the first semiconductor integrated circuit layer 201. Therefore, it is difficult to keep the diffused layer impurity distribution in the first semiconductor integrated circuit layer 201 precipitous, and it is difficult to structure an ultrafine semiconductor device on the first semiconductor integrated circuit layer 201. The above-described defect becomes the worst problem when the requirement to laminate elements whose power consumption is not very large as a memory cell array and with the same access rate, so that they have large capacity is to be met. In order to structure laminated semiconductor devices having the same access rate, it is required that they are manufactured under the same heat treatment condition and have the same characteristics, as well as the element form. However, as long as based on the above-described conventional manufacturing method, it is unavoidable that an excess high temperature heat treatment process is performed to the first semiconductor integrated circuit layer 201.

[0004] A technique in which two single crystal semiconductor substrates where a semiconductor device or a semiconductor integrated circuit device is structured are bonded and the one of them is thinned by polishing or the like in order to secure the crystallinity of the semiconductor thin film is disclosed in Y. Hayashi, et al., "Fabrication of Three-Dimensional IC Using Cumulatively Bonded IC (CUBIC) Technology" 1990 Symposium on VLSI Tech., p 95 (1990), for example. The cross-sectional view of a semiconductor device which is manufactured with this method is shown in Fig. 1. In Fig. 1, the numeral 2 is an insulating film for isolation between elements, 90 to 92 are electrodes connected with the semiconductor device, 94 and 95 are surface protection insulating films. Insulating adhesives 96 and 99, the hole 97, and a metal pool 93 are structured on the side of a second semiconductor substrate 101, and a metal bump 98 is structured on the side of a first semiconductor substrate 100.

[0005]

[Problem to be Solved by the Invention] In the above-described technology, although the semiconductor devices structured on the first semiconductor substrate 100 and the second semiconductor substrate 101 respectively are electrically connected with each other by the metal pool 93 and the metal bump 98, the thickness of the semiconductor substrate 100 or 101 used for manufacturing the semiconductor device is 500 μm or more, which is too thick to transmit ultraviolet or visible light, so the alignment between the hole 97 and the metal bump 98 is performed using infrared light whose wavelength is long and which can pass through the semiconductor substrate. Therefore, there is a drawback of the alignment accuracy, and pattern alignment of several μm or less is difficult. That is to say, aiming for connection between patterns of 1 μm or less, as the case of lamination of an ultrahigh-integrated high-density semiconductor device, has been impossible, from a viewpoint of commercialization.

[0006] The object of the present invention is to provide a high-performance ultrahigh-density integrated circuit device with excellent yield at a low price. And another object of the present invention is to remarkably improve the alignment accuracy in manufacturing a semiconductor device, and provide a manufacturing method of a semiconductor device, which can laminate large scale semiconductor integrated circuit layers with ultrahigh-accuracy in a longitudinal direction. Another object of the present invention is to provide equipment for substrate lamination, which can align SOI substrate with the accuracy of 10 to 100 times higher than the conventional case.

[0007]

[Means of Solving the Problem] The above-described objects are achieved by the following. A first semiconductor substrate where a first semiconductor integrated

circuit device is manufactured is bonded to another substrate, using a first adhesive. A first semiconductor integrated circuit device layer is formed by thinning the first semiconductor substrate from the rear surface side by means of grinding, polishing, or the like, and it is bonded to a transparent quartz substrate, using a second adhesive. In this condition, only the first adhesive is melted by a solvent of the first adhesive, and the first semiconductor integrated circuit device layer is transferred to the transparent quartz substrate. The first semiconductor integrated circuit device layer and a second semiconductor integrated circuit device or semiconductor integrated circuit device layer are aligned strictly and bonded together, using a third adhesive. For the alignment, when the first semiconductor integrated circuit device layer is structured to be thin enough, which is several μm or less, high-accuracy mask alignment equipment using ultraviolet rays as a light source can be used since the quartz substrate has transmissivity of 50 % with respect to ultraviolet rays and can transmit enough. A solvent of the second adhesive may be structured by a material which doesn't melt the third adhesive.

[0008] When the thinned semiconductor integrated circuit device layer is bonded to another semiconductor integrated circuit device or semiconductor integrated circuit device layer, it has to be considered that the pattern in the first stage is distorted about 1 μm per 10 cm due to intrinsic stress and thermal stress in the film by sequential film forming on the semiconductor substrate, which makes accurate alignment between semiconductor integrated circuit devices difficult. In order to correct the pattern distortion and perform accurate alignment and bonding, in the present invention, a technique in which external pressure is applied to the one or both of the substrates where the semiconductor integrated circuit device for which alignment should be performed is bonded so that the distortion is corrected is used, as a first technique. Furthermore, as another technique, a technique in which semiconductor integrated circuit devices having the same film formation structure as a cross section structure are bonded together is applied. In this case, the distortion extent caused by film formation is the same at any semiconductor integrated circuit device, and alignment defect by the distortion is dissolved. In the case where the semiconductor integrated circuit device layers bonded by the above-described technique are further bonded together, the cross section structure in each layer that is bonded further is made to be the same.

[0009]

[Function] According to the present invention, in the same way as manufacturing an ultrafine semiconductor integrated circuit device, high-accuracy mask alignment equipment using ultraviolet rays as a light source can be used, so that the lamination of

semiconductor integrated circuit devices is possible with the same high accuracy as that of manufacturing a conventional semiconductor integrated circuit device. Therefore, by using the technique of the present invention, even higher integrated semiconductor integrated circuit device can be realized with the conventional manufacturing equipment of a semiconductor device. Here, the manufacturing process is divided and only non-defective semiconductor layers are laminated to complete a semiconductor integrated circuit device. Therefore, manufacturing defect can be reduced greatly, compared to the conventional consistent manufacturing. That is to say, an ultrahigh integrated semiconductor integrated circuit device can be provided at a low price. In addition, it is possible that a structure element of the semiconductor integrated circuit device is structured separately on each semiconductor layer to be laminated, and a completed semiconductor integrated circuit device is made by the unification by lamination, therefore each semiconductor layer can be made and stored so that they can be laminated with a desired combination at a desired time. Therefore, it newly becomes possible to respond to the demand quickly. In addition, as the case of applying to a complementary transistor, a step of positional conversion of semiconductor layer conductivity type or the like can be omitted, which can reduce the number of manufacturing steps. According to the present invention, as semiconductor integrated circuit devices having the same semiconductor device region are laminated, even when a defective semiconductor device part exists, it can operate as a non-defective semiconductor integrated circuit device, by adopting a structure in which the defective part is not selected and a semiconductor device part in another layer is selected. That is to say, decrease in non-defective yield that grows as the area of a semiconductor integrated circuit device is enlarged can be greatly improved by the lamination structure. In addition to that, according to the present invention, complete isolation of structure elements is possible. Therefore, defectives such as a parasitic bipolar effect in a complementary transistor, that is, interference between adjacent elements such as a latch up phenomenon, malfunction based on α ray irradiation and the like can be dissolved almost perfectly. According to the present invention, a plurality of semiconductor integrated circuit devices whose heat treatment process is the same and having the same characteristics can be made to have ultra large capacitance by lamination.

[0010]

[Embodiments] The present invention will be described in further detail by embodiments hereinafter. Although drawings are used for the description convenience, main sections are shown being enlarged, so the case is required. Furthermore, in order

to simplify the description, the material of each part, the conductivity type of semiconductor layers and the manufacturing condition will be set and described. However, as for the material, the conductivity type of semiconductor layers and the manufacturing condition, the present invention is not limited to the embodiments, of course.

[0011] (Embodiment 1) Fig. 2 to Fig. 5 are cross-sectional views in which a first embodiment of a semiconductor integrated circuit device of the present invention is shown in order of the manufacturing process. A thermally-oxidized film of 200 nm thick is selectively formed in a desired part on the major surface of a single crystal silicon (Si) substrate 1 whose orientation is 100, resistivity 50 Ωcm, diameter 12.5 cm, and conductivity type p-type, using a known technique, so as to make an insulating film 2 for isolation between elements. Next, an Si thermally-oxidized film of 6 nm thick is formed on a substrate surface in a desired active region so as to make a gate insulating film 3. Then, after the gate insulating film in the desired region is removed selectively, a gate electrode 4 and a wiring electrode 9 formed of a laminated deposition film of a polycrystalline Si film and a tungsten silicide film are formed. Furthermore, after forming N-type low resistance diffused layers 6, 7 and 8, using the gate electrode 4 as a mask, an electrode protection insulating film 10 is deposited all over the surface (Fig. 2).

[0012] In the condition of Fig. 2, a molten wax 20 is applied to the electrode protection insulating film 10 all over the surface, and bonded to a transparent quartz substrate 30. Next, grinding is performed from the rear surface side of the Si substrate 1 by high accuracy grinding equipment to the thickness of 10 μm, and the Si substrate 1 is thinned to the surface defined by the rear surface of the insulating film 2 for isolation between elements, performing mechanical and chemical polishing. The above-described polishing is performed by pressing the Si substrate on an abrasive cloth provided on a rotating disk, with the pressure of 1.9×10^4 Pa, supplying an abrasive liquid added with ethylenediamine pyrocatechol. The polishing rate of the insulating film 2 for isolation between elements which is exposed as the polishing proceeds is extremely slow, compared to Si, and it is $1/10^4$ times or less. Therefore, the single crystal Si substrate 1 is perfectly planarized by the above-described polishing, and single crystal ultra-thin films Si of approximately 100 nm thick isolated from each other by the insulating film 2 for isolation between elements are obtained. After that, a protection insulating film 16 is formed on the polished surface (Fig. 3).

[0013] In the condition of Fig. 3, the alignment between the major surface of a second Si substrate 11 which is manufactured to be the condition of Fig. 2, prepared separately,

and the protection insulating film 16 is performed accurately, using the after-mentioned alignment equipment, and then they are laminated, using a fluorine resin as an adhesion layer 21. The thickness of the adhesive layer 21 is approximately 2 μm. After that, the second Si substrate 11 is heated to 100 °C so as to melt the wax 20, and it is released from the quartz substrate 30, then the residual wax is cleaned and removed with acetone. The wax removing step described above has no effect on the adhesive layer 21 which is formed of a fluorine resin (Fig. 4).

[0014] In this condition, a hole which penetrates through a terminal electrode 9 structured on the ultra-thin film Si layer 1, the insulating film 2 for isolation between elements, the adhesion layer 21, the electrode protection insulating film and the like on the Si substrate 11, and reaches a terminal electrode 15 on the Si substrate 11 is provided. And then a connection wiring 17 is formed by performing selective metal deposition to the hole. In addition, a wiring 18 which is based on a desired circuit structure is made, so that a semiconductor integrated circuit device is completed (Fig. 5).

[0015] As for the semiconductor integrated circuit device which is manufactured according to the above-described manufacturing method, the accuracy of the alignment between semiconductor layers structured is improved to be ± 0.5 μm, which is 10 times higher than the conventional laminated semiconductor integrated circuit device. By this, the interlayer connection can be made with the hole width 0.5 μm and the terminal electrode 15 width 1.5 μm. In this way, high integration can be achieved so that a basic circuit unit can be structured directly in the lamination direction without requiring the region that used to be required to form a bump or a pool for the interlayer connection. And the degree of freedom of circuit design can be greatly increased. The significant improvement in alignment accuracy in the lamination direction according to the present embodiment is based on the following: since a transparent semiconductor integrated circuit device layer formed of an ultra-thin film and transparent quartz can transmit ultraviolet rays, the alignment with a semiconductor integrated circuit device as a base, to which it is bonded, becomes possible with high accuracy.

[0016] Lamination of a semiconductor integrated circuit device layers formed of memory cell arrays as a semiconductor integrated circuit device according to the present invention is practiced, and each semiconductor integrated circuit device layer is manufactured by the manufacturing process of the same heat treatment. In addition, as for the function such as access rate, practically the same characteristics are obtained, without difference between each layer. In this way, improvement in non-defective rate

and improvement in operation speed due to the reduction of the maximum wiring length are achieved, compared to a conventional semiconductor integrated circuit device where memory cell arrays having the same capacitance are structured on the same plane surface.

[0017] As a common characteristic of a semiconductor integrated circuit device, transfer delay time can be used.

[0018] (Embodiment 2) Fig. 6 to Fig. 8 are cross-sectional views in which a semiconductor integrated circuit device according to a second embodiment of the present invention is shown in order of the manufacturing process. After a polycrystalline Si film 22 of 3 μm thick is deposited on an Si substrate 1 manufactured up to an electrode protection insulating film 10, according to the embodiment 1, the surface is planarized by performing mechanical polishing so that the mean square roughness is 0.3 nm or less. In this condition, it is bonded to a transparent quartz plate 30, using a molten wax 20, according to the embodiment 1. Then a single crystal ultra-thin film Si that is defined by the rear surface of an insulating film 2 for isolation between elements is formed by thinning from the rear surface of the Si substrate 1, and a protection insulating film 12 is formed on the rear surface (Fig. 6).

[0019] In the condition of Fig. 6, the alignment between the major surface of a single crystal Si substrate 11 which is separately manufactured up to the deposition of a thick polycrystalline Si film 24 and the planarizing polishing of the surface, using the same process as Fig. 6, and the protection insulating film 12 is performed accurately, using the after-mentioned alignment equipment, and then they are laminated, using a fluorine resin as an adhesive layer 23. The thickness of the adhesive layer 23 is approximately 0.5 μm (Fig. 7).

[0020] After that, the second Si substrate 11 is heated to 100 °C so as to melt the wax 20, and it is released from the quartz substrate 30, then the residual wax is cleaned and removed with acetone. And selective etching of the polycrystalline Si film 22 is performed. The wax removing step described above has no effect on the adhesion layer 23 which is formed of a fluorine resin. Next, on an electrode wiring 9 structured on a single crystal ultra-thin film Si layer 1, a hole which penetrates through an electrode wiring 9, the adhesion layer 23, the electrode protection insulating film and the like on the Si substrate 11, and reaches an electrode wiring 15 on the Si substrate 11 is provided, and an insulating treatment for the side wall of the hole is performed. And then, deposition of a metal film to the hole and pattern formation is performed so as to form a connection wiring 17. In addition, a wiring 18 which is based on a desired circuit structure is made, so that a semiconductor integrated circuit device is completed

(Fig. 8).

[0021] As for the semiconductor integrated circuit device which is manufactured according to the above-described manufacturing method, the accuracy of the alignment between semiconductor layers structured is improved to be ± 0.3 μm, which is 20 times higher than the conventional laminated semiconductor integrated circuit device. By this, the interlayer connection can be made with the hole width 0.4 μm and the width of the electrode wirings 15 and 17, 1.0 μm. In this way, high integration can be achieved so that a basic circuit unit can be structured directly in the lamination direction without requiring the region that used to be required to form a bump or a pool for the interlayer connection. And the degree of freedom of circuit design can be greatly increased. The significant improvement in alignment accuracy in the lamination direction according to the present embodiment is based on the following: since a transparent semiconductor integrated circuit device layer formed of an ultra-thin film and transparent quartz can transmit ultraviolet rays, the alignment with a semiconductor integrated circuit device as a base, to which it is bonded, becomes possible with high accuracy. Furthermore, the reason why the alignment accuracy is improved further, compared to the case of the embodiment 1, is considered to be that bonding can be performed without generation of bubbles even when the adhesion layer 23 is structured thin since the roughness on the surface to be laminated is planarized extremely.

[0022] (Embodiment 3) Fig. 9 to Fig. 11 are cross-sectional views in which a semiconductor integrated circuit device according to a third embodiment of the present invention is shown in order of the manufacturing process. A single crystal Si substrate 1 for which up to planarization polishing of the surface of a thick polycrystalline Si film 24 is performed according to the embodiment 2 is laminated on a mirror Si substrate 40 which is prepared separately, with a wax 25. After that, it is thinned from the rear surface side of the single crystal Si substrate 1, and an ultra-thin film single crystal Si layer is formed so that the film thickness is defined by the rear surface of an insulating film 2 for isolation between elements, according to the embodiment 1 (Fig. 9).

[0023] A polyvinyl alcohol film 26 which is a water-soluble adhesive is applied to the rear surface side of the ultra-thin film single crystal Si layer 1 manufactured up to the condition of Fig. 9, and it is laminated on a transparent quartz substrate 30. After that, the mirror Si substrate 40 is heated to 100 °C so as to melt the wax 25, and it is released from the quartz substrate 30, then the residual wax is cleaned and removed with acetone. The polyvinyl alcohol film 26 is not affected at all by the acetone cleaning (Fig. 10).

[0024] A separately prepared single crystal Si substrate 11 for which up to planarization polishing of the surface of a thick polycrystalline Si film 27 is performed

according to the embodiment 2 is laminated on the ultra-thin film single crystal Si layer 1 in the condition of Fig. 10, with their polycrystalline Si surfaces laminated directly to each other. As for the lamination described above, alignment of each other is performed according to the after-mentioned accuracy alignment equipment, in the same way as the embodiment 2. N-type low resistance diffused layers 6, 7 and 8 are formed on the single crystal Si substrate 11 in advance, according to the embodiment 1 described above. After the above-described direct lamination, the single crystal Si substrate 11 is soaked in water so as to melt the water-soluble adhesive 26, and is released from the transparent quartz substrate 30. Then a heat treatment to improve the adhesive strength is performed under the condition of 900 °C, 30 minutes. After that, a gate insulating film is formed on the surface of the single crystal ultra-thin film Si layer 1, and then a hole is made on an insulating film 2 for isolation between elements where a gate electrode 4 is extended. In addition, a second gate electrode 13 is formed on the single crystal ultra-thin film Si layer 1 so as to correspond to the gate electrode 4, and low resistance diffused layers 61, 62, 63 and the like are formed, using the second gate electrode 13 as a mask. Next, on an electrode wiring 9 structured on the single crystal ultra-thin film Si layer 1, a hole which penetrates through the electrode wiring 9, the polycrystalline Si layers 24 and 27, an electrode protection insulating film and the like on the Si substrate 11, and reaches an electrode wiring 15 on the Si substrate 11 is provided, and an insulating treatment for the side wall of the hole is performed. And then, deposition of a metal film to the hole and pattern formation are performed so as to form a connection wiring 17. In addition, a wiring 18 which is based on a desired circuit structure and an electrode protection insulating film 10 are formed, so that a semiconductor integrated circuit device is completed (Fig. 11).

[0025] As for the semiconductor integrated circuit device which is manufactured according to the above-described manufacturing method, the accuracy of the alignment between semiconductor layers structured is improved to be ± 0.3 μm, which is 20 times higher than the conventional laminated semiconductor integrated circuit device. In this way, high integration can be achieved so that a basic circuit unit can be structured directly in the lamination direction without requiring the region that used to be required to form a bump or a pool for the interlayer connection. And the degree of freedom of circuit design can be greatly increased. The significant improvement in alignment accuracy in the lamination direction according to the present embodiment is based on the following: since a transparent semiconductor integrated circuit device layer formed of an ultra-thin film and transparent quartz can transmit ultraviolet rays, the alignment

with a semiconductor integrated circuit device as a base, to which it is bonded, becomes possible with high accuracy.

[0026] In addition, as for a semiconductor integrated circuit device according to the present embodiment, a technique of laminating directly without using an adhesive is used, so that the gate electrode 13, the diffused layers 61 to 63 and the like can be manufactured after the lamination. Therefore, a semiconductor integrated circuit device layer to be laminated can be structured so that its current control is performed from the top and bottom of the ultra-thin film Si layer, and a large current of more than three times the conventional structure transistor structure, that is, speeding up becomes possible, along with ultrahigh integration in a longitudinal direction.

[0027] (Embodiment 4) Fig. 12 is a cross-sectional view in which a semiconductor integrated circuit device according to a fourth embodiment of the present invention is shown. In the embodiment 3, a semiconductor substrate 31 on which a semiconductor integrated circuit device layer 1 of an ultra-thin film manufactured according to the technique described in the embodiment 3 is laminated directly is used, instead of a semiconductor substrate 11 on which the semiconductor integrated circuit device layer 1 should be laminated. A gate electrode 19, another electrode and the like are structured on the semiconductor integrated circuit device layer 1 in advance. Although the mirror Si substrate 40 and the single crystal Si substrate 1 are bonded with the wax 25 in Fig. 9, the major surface of the mirror Si substrate 31, on which a thermally-oxidized film 29 is formed, and the surface of a polycrystalline Si film 28 on a single crystal Si substrate 1, for which planarization polishing is performed are bonded together directly without using an adhesive, as for a semiconductor integrated circuit device of the present embodiment. After that, a heat treatment to improve the adhesive strength is performed under the condition of 900 °C, 30 minutes, and it is thinned from the rear surface side of the single crystal Si substrate 1, and the semiconductor integrated circuit device layer 1 whose thickness is defined by the bottom surface of an insulating film 2 for isolation between elements is formed. After that, a gate insulating film is formed on the new major surface of the semiconductor integrated circuit device layer 1, and a hole is provided in a desired part of the insulating film 2 for isolation between elements region. Then, a low resistance diffused layer is formed by self-alignment with an electrode including a gate electrode 5 and the gate electrode 5. Next, an electrode protection insulating film and a thick polycrystalline Si film are deposited all over the surface, and the surface of the polycrystalline Si film is polished so as to be planarized. The surface of the polycrystalline Si film on the semiconductor substrate 31, manufactured according to the technique described above, and a polycrystalline Si

surface of a separately prepared ultra-thin film semiconductor integrated circuit device layer 1 (Fig. 10) where a gate electrode 4 and the like laminated on a quartz substrate 30 using polyvinyl alcohol as an adhesive 26 are structured are laminated directly without an adhesive. In the laminating process described above, the alignment between ultra-thin film semiconductor integrated circuit device layers is performed using the after-mentioned accuracy alignment equipment, in the same way as the above-mentioned embodiment 2 and 3. After the laminating process, release of the transparent quartz substrate 30 by removing the adhesive 26 using polyvinyl alcohol, a heat treatment for improving the adhesive strength, and formation of a second gate electrode 13, a diffused layer and the like on the laminated single crystal ultra-thin film Si layer are performed according to the above-described embodiment 3. In this condition, a hole which penetrates through the diffused layer formed on the single crystal ultra-thin film Si layer which is exposed on the major surface, the polycrystalline Si layer which is structured on the bottom, and the like and reaches the electrode on the single crystal ultra-thin film Si layer which is buried is provided. Last, after an insulating treatment of the polycrystalline Si side face, selective formation of a metal film in the hole, formation of a wiring based on a desired circuit structure and an electrode protection insulating film are performed so as to complete a semiconductor integrated circuit device (Fig. 12).

[0028] As for the semiconductor integrated circuit device manufactured according to the manufacturing method described above, as is the case with a semiconductor integrated circuit device according to the above-described embodiment 3, the alignment accuracy between semiconductor layers structured is improved 20 times or more, compared to a conventional laminated semiconductor integrated circuit device, and the region that used to be required to form a bump or a pool for the interlayer connection can be omitted. In this way, high integration can be achieved so that a basic circuit unit can be structured in the lamination direction, and the degree of freedom of circuit design can be greatly increased. The significant improvement in alignment accuracy in the lamination direction according to the present embodiment is based on the following: since a transparent semiconductor integrated circuit device layer formed of an ultra-thin film and a transparent quartz substrate can transmit ultraviolet rays, the alignment with a semiconductor integrated circuit device as a base, to which it is bonded, becomes possible with high accuracy.

[0029] In addition, as for the semiconductor integrated circuit device according to the present embodiment, any of the laminated semiconductor integrated circuit device layer used the technique of laminating directly without using an adhesive, so that a structure

which needs a high temperature heat treatment, such as formation of a diffused layer, can be provided after a lamination bonding process. By this, structuring gate electrodes for current control on the top and bottom of the semiconductor layer, as for any layer of a laminated semiconductor integrated circuit device layer, becomes possible, and higher operation, compared to the semiconductor integrated circuit device of the above-described embodiment 3, is achieved further. That is to say, ultrahigh integration and ultrahigh speeding due to lamination can be achieved at the same time, compared to a semiconductor integrated circuit device of the conventional structure.

[0030] (Embodiment 5) Fig. 13 is a cross-sectional view in which a semiconductor integrated circuit device according to a fifth embodiment of the present invention is shown. In the above-described embodiment 4, in the formation of the ultra-thin film semiconductor integrated circuit device layer 1 to be laminated directly on the semiconductor substrate 31, before the polycrystalline Si film 28 which structures the laminating surface with the semiconductor substrate 31 is deposited, a desired hole is provided in the electrode protection insulating film on a terminal part 7 to which a ground potential is applied, and a first laminated film 42 of a low resistance polycrystalline Si film and a tungsten (W) silicide film is formed all over the surface. After that, a second electrode protection insulating film is deposited on the whole surface, and then deposition of a polycrystalline Si film 28, the planarizaion polishing and the like are performed according to the embodiment 4 described above. In addition, in the manufacturing step of the above-described embodiment 4, after forming the gate electrode 13, when providing a hole which penetrates through the upper ultra-thin film semiconductor integrated circuit device layer, a hole which penetrates through a base ultra-thin film semiconductor integrated circuit device layer in the terminal part to which a ground potential is applied in the upper ultra-thin film semiconductor integrated circuit device layer and reaches a laminated film 42 is provided, and it is filled with a metal film for connection. Furthermore, in the manufacturing process of the above-described embodiment 4, after the electrode protection insulating film 41 is deposited on the major surface of the upper ultra-thin film semiconductor integrated circuit device layer, a hole is provided in a desired terminal part 62 of the upper and under ultra-thin film semiconductor integrated circuit device layers, to which a power source potential is applied. Then, a second laminated film 43 of a low resistance polycrystalline Si film and a tungsten (W) silicide film is formed all over the surface again. Last, a connection is made in a desired part so that a ground potential and a power source potential are applied to the first and the second laminated films 42 and 43 respectively (Fig. 13).

[0031] The semiconductor integrated circuit device which is manufactured according to the manufacturing method described above has the characteristics of ultrahigh integration in the lamination direction and ultrahigh speeding of the semiconductor integrated circuit device according to the above-mentioned embodiment 4, as well. In addition, as for the semiconductor integrated circuit device according to the present embodiment, higher operation, compared to the embodiment 4, can be achieved. In the semiconductor integrated circuit device of the present embodiment, any of the power source voltage applied terminal and the ground potential applied terminal on the chip is connected with the conductive layer structured in the form of a sheet in almost the whole region on the top and bottom of the semiconductor integrated circuit device layer. Because of this, the ground resistance and the power source resistance are defined by the layer resistance from the voltage supply point to each terminal, so that the ground resistance and the power source resistance can be greatly reduced, compared to the case in which the ground resistance and the power source resistance are defined by the wiring resistance based on the effective length and width of the wiring which is extended from the voltage supply point to each terminal, as the conventional semiconductor integrated circuit device. The reducing effect of the ground resistance and the power source resistance has more efficiency as the area occupied by the semiconductor integrated circuit device is enlarged.

[0032] (Embodiment 6) In the embodiment 5, only an n-channel MOS transistor is structured on the ultra-thin film semiconductor integrated circuit device layer to be directly laminated on the semiconductor substrate 31 with the polycrystalline Si film 28 therebetween, and only a p-channel MOS transistor is structured on the ultra-thin film semiconductor integrated circuit device layer that is structured in lamination on the upper part of the ultra-thin film semiconductor integrated circuit device layer, and a semiconductor integrated circuit device made of a complementary MOS transistor is manufactured with a laminated structure. The numeral 7 is a ground potential applied terminal, and 62 is a power source potential applied terminal. The connection of the n-channel and the p-channel transistors for the complementary MOS transistor is made by an interlayer connection wiring 17 between ultra-thin films.

[0033] As for the semiconductor integrated circuit device manufactured according to the manufacturing method described above, the n-channel MOS transistor and the p-channel MOS transistor are structured on different ultra-thin films. Therefore, the manufacturing process in which a semiconductor substrate is separated to make regions where transistors of each conductivity type are structured (it is called well region) and the occupied region for that can be omitted. In this way, reduction of the

manufacturing cost and even higher integration can be achieved. In addition, the transistors having different conductivity type are completely separated from each other, with different layers, so that mutual interference between adjacent elements, such as a latch-up phenomenon is completely dissolved.

[0034] (Embodiment 7) Fig. 14 to Fig. 15 are cross-sectional views in which a semiconductor integrated circuit device according to a seventh embodiment of the present invention is shown in order of the manufacturing process. Slots of a desired pattern are formed from the major surface side of a p-type low resistance Si substrate 31, and a thin insulating film 32 is formed on the side wall of the slots by thermal oxidation. Then, a low resistance polycrystalline Si film 33 added with an impurity is deposited on the whole surface so as to fill the slots. After that, mechanical polishing is performed to planarize the major surface, and the polycrystalline Si film 33 region is structured separated from the Si substrate 31 (Fig. 14).

[0035] Here, an insulating film for isolation between elements, gate electrodes 46 and 47, an n-type low resistance diffused layer, an electrode protection insulating film and the like according to a desired circuit structure are formed on a separately prepared single crystal Si substrate 1 of p conductivity type, and then an ultra-thin film single crystal semiconductor integrated circuit device layer 1 whose thickness is defined by the bottom surface of the insulating film for isolation between elements is formed, according to the embodiment 1. The above-described ultra-thin film is bonded to the Si substrate 31 manufactured up to Fig. 14, based on the accurate alignment, according to the embodiment 1. The bonding is performed using a coating film of a fluorine resin as an adhesive 34. After that, the transparent quartz substrate used for the alignment is removed, and a hole is provided in an ultra-thin film Si layer in a desired diffused layer region and the adhesive layer 34 just beneath. Then, an electrode 49 to electrically connect the separated polycrystalline Si film 33 and the desired diffused layer region is formed. Next, an electrode protection insulating film is deposited on the whole surface, and a hole and a wiring electrode 14 which structures a bit line are formed for the connection with a desired diffused layer region 48, so that a semiconductor memory device with one capacitance element and one transistor as a basic unit (Fig. 15).

[0036] As for the semiconductor integrated circuit device manufactured according to the manufacturing method described above, the semiconductor substrate where the capacitance element is structured and the semiconductor substrate where the control transistor is structured are manufactured separately and then integrated together by lamination, so that restrictions of the manufacturing process and the layout, concerning

manufacturing a capacitance element, are greatly eased. Therefore, the depth of the slot formed on the Si substrate 31 and the slot area which can be extended to the bottom of the transistor can be set to be desired values, so that a large enough capacitance value can be realized for a memory capacitance element part. In this way, malfunction based on α ray irradiation can be dissolved dramatically.

[0037] (Embodiment 8) Fig. 16 is a cross-sectional view showing a semiconductor integrated circuit device according to an eighth embodiment of the present invention. In the present embodiment, a semiconductor substrate 35 where a thermally-oxidized film 36, a refractory metal silicide film 37 on the thermally-oxidized film 36, which is patterned corresponding to a desired circuit structure, and a low resistance polycrystalline Si film 38 deposited all over the surface on the refractory metal silicide film are structured on the major surface is used, instead of the Si substrate 31 on which a capacitance element should be structured in the embodiment 7. The refractory metal silicide film 37 may be structured all over the surface without patterning, depending on the desire. Here, formation of a slot for a capacitance element is performed in the polycrystalline Si film 38 region, and after formation of a thin insulating film on the processed surface, the slot region is filled with a low resistance polycrystalline Si film 33. After that, the polycrystalline Si films 33, 36 and the like on the major surface of the semiconductor substrate 35 are planarized by mechanical polishing. Then, the planarized surface and the ultra-thin film Si layer are bonded together according to the embodiment 7, and the manufacturing process after that is continued, so that a semiconductor integrated circuit device is manufactured (Fig. 16).

[0038] As for the semiconductor integrated circuit device manufactured according to the manufacturing method described above, the polycrystalline Si film 38 which structures one electrode of the capacitance element is connected with the refractory metal silicide film 37 with even lower resistance electrically, and it can follow at a faster pace with respect to application of a plate potential. By this, the speed of reading and writing of memory can be further increased, compared to the semiconductor integrated circuit device of the embodiment 7.

[0039] (Embodiment 9) Fig. 17 is a cross-sectional view showing a semiconductor integrated circuit device according to a ninth embodiment of the present invention. In the present embodiment, lamination of semiconductor integrated circuit devices according to the embodiment 2 is repeated and a semiconductor integrated circuit device with a multilayer structure is manufactured. In Fig. 17, the numeral 11 is a semiconductor support substrate, 50 is a first ultra-thin film Si layer structuring a main storage. The numerals 51, 52 and 53 are a second, a third and a fourth ultra-thin film

Si layers and each of them structures an extended storage.

[0040] As for the semiconductor integrated circuit device according to the present embodiment, increase in arithmetic processing time due to wiring delay in a conventional semiconductor integrated circuit device can be greatly reduced, by the effect of lengthwise high integration due to an accurate alignment lamination structure.

[0041] (Embodiment 10) In the present embodiment, as the 51, 52 and 53 of the embodiment 9, a cache storage is structured. The semiconductor device to structure the cache storage is made by an ultrahigh-speed bipolar transistor. A main storage 50 is structured by a MOS transistor.

[0042] As for the semiconductor integrated circuit device according to the present embodiment, exchange of the storage data between the cache storage and the main storage is possible instantaneously, by the effect of lengthwise high integration due to an accurate alignment lamination structure, therefore a cache storage of large capacity can be provided. By this, operation speed of the whole storage can be greatly increased, and information of large capacity can be stored.

[0043] (Embodiment 11) Fig. 18 is a cross-sectional view showing a semiconductor integrated circuit device according to an eleventh embodiment of the present invention. In the present embodiment, lamination of semiconductor integrated circuit devices according to the embodiment 10 is repeated and a semiconductor integrated circuit device with a multilayer structure is manufactured. In Fig. 18, the numeral 54 is a central processor, 50 is a main storage, 51 to 53 are an order processor, a system control device, an input-output processor, an extended storage and the like, and these are laminated in a plurality of layers according to the embodiment 2, so that a semiconductor integrated circuit device structuring an ultrahigh-speed computer.

[0044] As for the semiconductor integrated circuit device according to the present embodiment, the connection length between devices is extremely decreased, by the effect of lengthwise high integration due to an accurate alignment lamination structure. By this, the number of times order processing is made per 1 second can be greatly increased, compared to a conventional large computer made by assembling semiconductor devices and the like.

[0045] (Embodiment 12) Fig. 19 and Fig. 20 are cross-sectional views showing a semiconductor integrated circuit device according to a twelfth embodiment of the present invention. A first technique of the present embodiment is shown in Fig. 19, and a second technique is shown in Fig. 20. Fig. 19 is a semiconductor integrated circuit device of the present embodiment, manufactured according to the same manufacturing method as the embodiment 2, and semiconductor integrated circuit

device layers having the same function are aligned top and bottom and structured by lamination. Furthermore, a transistor to control the current path is placed serially for each desired unit circuit in each semiconductor integrated circuit device layer. The numerals 55 and 56 are gate electrodes of the transistor in each of the adjacent semiconductor integrated circuit device layers.

[0046] As for the semiconductor integrated circuit device according to the present embodiment, non-defective yield that decreases as the area and the scale of a semiconductor integrated circuit device are enlarged can be improved. That is, in the case where a desired unit circuit in any of the laminated semiconductor integrated circuit device layers has a defect, the path is blocked by the transistor which is connected in series with the defective circuit (a transistor which is controlled by the gate electrode 55, for example), and a transistor (a transistor which is controlled by the gate electrode 56, for example) is made conductive so as to select only the path on the side of a non-defective desired unit circuit. In this way, the situation in which the existence of a defective circuit in one part makes the semiconductor integrated circuit device defective and the non-defective yield is greatly decreased can be greatly improved, which paved the way for further enlargement of the area and the scale of a semiconductor integrated circuit device. The defective part in each semiconductor integrated circuit device layer is checked by measurement beforehand in the stage where each semiconductor integrated circuit device layer is formed, and then lamination is made.

[0047] Another technique of the present embodiment is a semiconductor integrated circuit device shown in Fig. 20, and semiconductor integrated circuit device layers having the same function are aligned top and bottom and structured by lamination, according to the embodiment 4. The difference from the embodiment 4 is as follows: after manufacturing each semiconductor integrated circuit device layer, a defective part in the desired unit circuit is identified by electrical measurement, and the current path of the defective unit circuit (the indicated region of the upper semiconductor integrated circuit device layer in Fig. 20, for example) is broken by a laser beam which is finely narrowed, so as to make a region 39 which is in an electrically open state. By this, by this, as for the semiconductor integrated circuit device in Fig. 20, a structure in which the path on the side of a non-defective desired unit circuit (the indicated region of the under semiconductor integrated circuit device layer in Fig. 20, for example) is selected via a connection wiring electrode 17, as the current path, is realized. That is, the same relief of a defective unit circuit part as the case of another technique of the present embodiment shown in Fig. 19 becomes possible. As for the present technique, the

extra transistor required for relief of a defective unit circuit is not needed, therefore increase in the occupied area can be avoided and the enlargement of the area and scale of a semiconductor integrated circuit device can be further promoted, compared to the semiconductor integrated circuit device shown in Fig. 19.

[0048] (Embodiment 13) Fig. 21 and Fig. 22 are schematic diagrams showing manufacturing equipment of a semiconductor integrated circuit device of the present invention. The semiconductor integrated circuit device in each embodiment described above is manufactured using the manufacturing equipment of the present embodiment. In order to align two semiconductor substrates or semiconductor thin films 75 and 76, on which a pattern is formed, with high accuracy, and bond them to each other, it is needed to correct the expansion and contraction, distortion or the like unique to each semiconductor substrate or semiconductor thin film, based on the film formation, so that they are aligned to each other with high accuracy. In Fig. 21, a second stage 72 and a third stage 73 are placed on a first stage 71. A substrate 75 and a substrate 76 are vacuum-contacted to the stage 72 and the stage 73, respectively. Each substrate is conveyed to the stage, in the condition of being relatively pre-aligned to the stage. A regular automatic conveying mechanism is used for conveying the substrate. The stage 72 and the stage 73 have a rolling mechanism respectively, and the chip arrangement on the substrate can be set to be parallel to the movement axis of the stage. A target mark for orientation is formed on the substrate, and position detection of the target mark is performed by position detecting optical systems 77 and 78. In this equipment, it is structured to align the substrate 76 with respect to the substrate 75. The relative position error of the substrate 75 and the substrate 76 is measured by the position detecting optical systems 77 and 78. When there is a position error, the substrate 76 is deformed by a substrate deformation mechanism on the stage 73 and controlled so that there is no position error between the substrates 75 and 76. Segmentalized substrate absorption blocks are placed on the stage 73, and each block 74 is structured so as to be able to move by itself by a piezo element. The position of the substrate is perceived relatively with respect to stage marks 80 and 81. The substrate 75 and the substrate 76 have positional relation of mirror reversal, and the positional relation of them are data-processed in a computer control system 83, based on the information from a position perception part 79. The data is processed in a substrate deformation control mechanism 82, and the segmentalized substrate absorption blocks 74 are moved, so that the substrate 76 is deformed. By this operation, the same formation can be made, in the condition where the substrate 76 is mirror-reversed with respect to the substrate75.

[0049] In the next step, as shown in Fig. 22, the substrate 75 is mirror-reversed in the condition of being fixed to the stage 72, and moved so that the major surface of the substrate 76 and the major surface of the substrate 75 face each other. A movement mechanism is not shown in the figure, but a regular arm-type moving mechanism is used. In this condition, position of the stage marks 80 and 81 is detected using a position detecting optical system 84. The data is processed in the computer control system 83. This data is processed in a stage position control system 85, and the stage 73 is moved by a movement mechanism 86 and positioned relatively to the stage 72. After that, the substrate 72 is lowered by a vertical movement mechanism of the stage 72 and attached to the substrate 73, which completes the lamination. To perform the lamination well, slight tilt of the stage 72 can be set. By the series of operations described above, the substrate 75 and the substrate 76 having different deformation can be corrected to have the same formation and laminated. In the embodiment described above, a mechanism of moving the segmentalized substrate absorption block 74 by a piezo element is used for the deformation mechanism of the substrate 76, but another technique may be used. A method in which the absorption block 74 is moved by a thermal deformation plate, a method in which the position is changed by using pressure of liquid or gas, or the like is possible, for example. That is, feature of the present equipment is having a mechanism which can deform the formation of a substrate freely. Here, function of the equipment is described, segmentalizing the equipment. However, feature of the manufacturing equipment of the present embodiment is the same, when Fig. 21 and Fig. 22 are in the same equipment or they are structured as different pieces of equipment. Furthermore, although the description of mechanisms that are not directly related to the feature of the manufacturing equipment of the present embodiment is omitted, mechanisms required for regular position alignment equipment are added. A temperature control mechanism for the whole equipment, a stage position length measurement mechanism, a substrate cassette-to-cassette conveying mechanism and the like are the examples. In addition, as the other version of the present equipment, it is possible to measure the deformation of the chip arrangement from the rear surface of the substrate 75, as shown in Fig. 22. In the case where the deformation of the substrate 76 is measured, the stage 72 needs to be taken to the position which doesn't disturb the detection. In this case, the stage 71 in Fig. 21 is not needed, so that the miniaturization of the equipment is achieved. The substrate 75 or 76 which uses the manufacturing equipment of the present embodiment doesn't need to be limited to a regular single crystal semiconductor substrate where a semiconductor integrated circuit device is manufactured, and it may be a semiconductor integrated

circuit device layer which is manufactured on a single crystal ultra-thin film Si film laminated by an adhesive on a semiconductor substrate as a support substrate, as described in the embodiment 1 and the like. The above-described single crystal ultra-thin film Si film may be laminated directly, without using an adhesive. In this case, after accurate alignment, adhesion and bonding according to the present embodiment are performed between semiconductor integrated circuit device layers, the substrates 75 and 76 are removed from the manufacturing equipment of the present embodiment and soaked in a solvent of the adhesive, so that the support substrate is detached. In the case of direct lamination without using an adhesive, the support substrate is removed by grinding, polishing or the like.

[0050] (Embodiment 14) In the embodiment 13, as shown in Fig. 21, position detection using the position recognition target on the substrates 75 and 76 is performed in the condition where the major surface of the substrates 75 and 76 faces upward. In the present embodiment, by structuring the substrate 75 and the second stage 72 so as to be able to transmit visible light and ultraviolet rays, it is performed in the condition where the substrate 75 is mirror-reversed, that is, the substrate 75 and 76 are kept where they are, as shown in Fig. 22. The recognition may be performed between the position recognition target marks on the substrate 75 and the substrate 76, omitting the second stage 72. Here, the position recognition target mark on the substrate 76 is identified by the detecting optical system 77, passing through the substrate 75. According to the present embodiment, the alignment mechanism between substrates by the stage marks 80 and 81 used in the embodiment 13 can be omitted, and even more direct alignment between the substrates 75 and 76 becomes possible, so that simplification of the equipment is achieved. Furthermore, in the embodiment 13, disadvantage that position recognition becomes impossible arises in the case where substantial position unconformity exists between the substrate 75 and the second stage 72. However, in the present embodiment, the existence of substantial position unconformity between the substrates 75 and 76 is quite obvious, and can be corrected easily.

[0051] In the present embodiment, by structuring the substrate 75 and the second stage 72 so as to transmit ultraviolet rays, the detecting optical system 77 of shorter wavelength, compared to the case where only infrared rays are transmitted as the case of a regular Si substrate, can be used. Therefore, more accurate position detection is possible. It is preferable that the second stage 72 is a transparent quartz substrate, considering the transmitting characteristic of ultraviolet rays and the availability, and the substrate 75 is a semiconductor integrated circuit device layer of a single crystal Si ultra-thin film laminated by a thin adhesive (especially a fluorine resin adhesive, which

can transmit ultraviolet rays) on the transparent quartz substrate. Here, the thickness of the Si ultra-thin film is preferably 100 nm or less, for transmitting ultraviolet rays. As for the substrates 75 and 76 for which processes of accurate position detection, the bonding after that, and ultra-thinning of the film and the like are performed according to the present embodiment, the transparent quartz substrate is removed according to the embodiment 1 or 2, so that an ultra-thin film is formed.

[0052] In the embodiments 13 and 14, the factor of interfering the accurate alignment between the substrates 75 and 76 is based on film formation on the substrate, which is essential to manufacturing an integrated circuit device structured on the substrate 75 and 76 respectively. That is, because of internal stress that various insulating films and metal films formed on the substrate themselves have and thermal stress based on the difference in coefficient of thermal expansion from the substrate, caused by various heat treatments performed in the condition of film formation on the substrate, the substrate where a semiconductor integrated circuit device or a semiconductor integrated circuit device layer is structured produces warpage so as to be concave or convex to the top. In this way, distortion, expansion and contraction are caused on the pattern on the substrate surface. The above-described distortion, expansion and contraction of the pattern are especially pronounced in the adjacent region of the substrate. In the step of performing accurate alignment between two substrates, in order to substantially reduce the effect of the above-described distortion, expansion and contraction of the pattern, it is solved when the warpage on the two substrates where integrated circuit devices are manufactured is controlled uniformly. As one of the techniques, the two substrates are structured to be plane respectively. Specifically, although the substrate 75 is vacuum-contacted to the stage 72 and the substrate 76 is vacuum-contacted to the stage 73 in the embodiments 13 and 14, the vacuum contact can be realized by absorbing the substrate strongly by the stage having many absorption holes and whose surface is extremely flat. As more absorption holes are structured, the absorption substrate can correspond with the shape of the stage well, so the stage with a porous structure is preferable. By this, the major surfaces of the two substrates for which accurate alignment is performed can be kept flat, and the distortion, expansion and contraction of the pattern can be minimized. From a viewpoint of controlling the distortion, expansion and contraction of the pattern on the major surface of the two substrates, the major surfaces are not necessarily plane, and they may be controlled to be desired curved surfaces so that the distortion, expansion and contraction are the same.

[0053] (Embodiment 15) Fig. 23 is a cross-sectional view in which a manufacturing method of a semiconductor integrated circuit device according to a fifteenth

embodiment of the present invention is shown. In the present embodiment, a technique in which the accuracy of the alignment between the two substrates is stricter is pursued. As described above, the distortion, expansion and contraction of the pattern formed on the substrate surface depend in good part on the thickness of various insulating films and metal films formed on the substrate in the manufacturing process of an integrated circuit device and heat treatment history after the formation of various films. Therefore, it is, in a manner, unavoidable that distortion, expansion and contraction specific to the integrated circuit device arise on the pattern of the integrated circuit device formed on the semiconductor substrate. Reflecting the above-described situation, in the present embodiment, two substrates are laminated, assuring the accurate alignment. That is to say, the two substrates to be laminated have the same past records such as the film formation condition. In Fig. 23, 57 and 56 are semiconductor integrated circuit device layers of single crystal Si ultra-thin films respectively, and they are ultra-thinned and laminated according to the embodiment 2 or 3. The numeral 30 is a transparent quartz substrate, and it is bonded to an ultra-thin film 57, by using a water-soluble adhesive 26 and a fluorine adhesive 34. The manufacturing process of 57 and 58 are different, and the amounts of warpage of the semiconductor substrates are different from each other in the step before ultra-thinningof the film, that is, the step in which the semiconductor integrated circuit device is formed on the major surface of the semiconductor substrate. For such semiconductor substrates, in the present embodiment, an insulating film having different coefficient of linear expansion from that of the semiconductor substrate is deposited so that the direction and amount of the warpage of the two semiconductor substrates are controlled to be the same. The deposition of the insulating film described above may be performed on any surface of the semiconductor substrate. After that, accurate alignment and bonding of the two semiconductor substrates are performed, using the equipment described in the embodiment 13. The amounts of distortion, expansion and contraction of the pattern are almost equal between the two substrates with the same direction and amount of the warpage. Therefore, relative pattern misalignment is resolved, and good alignment can be performed.

[0054] Two ultra-thin films 57 and 58 manufactured by the same manufacturing processes are bonded to the transparent quartz substrates 30 respectively, and they are laminated directly without using an adhesive, using the equipment described in the embodiment 13 again, so that an ultra-thin film of four-layered structure is made. After that, one of the transparent quartz substrates 30 is removed by melting the water-soluble adhesive 26, and the rest is bonded to a separately prepared support

substrate. Then, the other transparent quartz substrate 30 is also removed by melting the adhesive 34, so that a semiconductor integrated circuit device is completed. In manufacturing the above-described ultra-thin film of four-layered structure, the overlapping two ultra-thin films 57 and 58 are manufactured by exactly the same manufacturing processes, and have the same cross section structures. By this, pattern misalignment generated on the overlapping two ultra-thin films 57 and 58 is relatively equal, and correct alignment can be realized easily without a special measure.

(Embodiment 16) Fig. 24 is a plan view in which a manufacturing method of a semiconductor integrated circuit device according to a sixteenth embodiment of the present invention is shown. In each embodiment described above, description of a semiconductor integrated circuit device of the present invention, including the manufacturing method, is made. In any of the embodiments, a technique in which a semiconductor integrated circuit device or a semiconductor integrated circuit device layer is once bonded to a semiconductor substrate, a quartz substrate or the like that is separately prepared, and after performing desired manufacturing processes such as ultra-thinning of a film, the ultra-thin film is laminated on another substrate again by some method is used. In the technique described above, a semiconductor substrate, a quartz substrate or the like bonded first is released from a semiconductor integrated circuit device or a semiconductor integrated circuit device layer, and the release by a solvent is sometimes difficult, depending on the adhesive. This is because the thickness of the adhesive is small and the solvent doesn't spread into the adhering surface quickly. In order to spread the solvent into the adhering surface quickly and release the quartz substrate 72 from the semiconductor integrated circuit device or the semiconductor integrated circuit device layer 75 quickly, in the present embodiment, as shown in Fig. 24, the quartz substrate 72 having a plurality of microscopic through-holes 59 penetrating from the back face to the front face, formed in a desired part of the quartz substrate 72 to be released is used. Responding to the type of the adhesive, the number of through-holes 59 may be one.

[0055] In the manufacturing processes of a semiconductor integrated circuit device according to the embodiment 1, 2 and the like, after a semiconductor substrate on which a semiconductor integrated circuit device or a semiconductor integrated circuit device layer is formed is bonded to a quartz substrate and desired manufacturing processes such as ultra-thinning of a film are performed, it is accurately aligned with and bonded to another semiconductor integrated circuit device or semiconductor integrated circuit device layer which is separately prepared. After that, the quartz substrate is released. In this releasing step, the comparison of the times required for the release between the

quartz substrate 72 according to the present embodiment and the quartz substrate 30 having no through-hole 59 is made. Various cases using a water-soluble adhesive such as polyvinyl alcohol or a fluorine adhesive as the adhesive to be melted, setting the diameter of the through-hole 59, provided on the quartz substrate 72, from 10 μm to 200 μm, and setting the number of through-holes 59 from 1 to 50 are studied. In any case, the one using the quartz substrate 72 with the through-hole 59 according to the present embodiment can shorten the time required for the release greatly to 1/10 or less. The quartz substrate 72 having the through-hole 58 of the above-described condition can operate exactly the same with the case of a quartz substrate having no through-hole 59, through the desired manufacturing processes such as bonding beforehand and ultra-thinning of a film after that, and there is no problem.

[0056] Although the materials of the adhesive are specified in order to simplify the description in each embodiment described above, the spirit of the present invention is that the second adhesive is not melted when the first adhesive is melted. Therefore, the material of the adhesive is not limited at all, as long as it is within the condition above. In addition, melting of the adhesive is a step for enabling the manufactured ultra-thin film to be transferred to another support substrate. Therefore, when the rise in manufacturing cost by consumption of the adherend substrate is not considered, the adherend substrate may be removed by mechanical polishing and grinding after the ultra-thin film is transferred to another support substrate.

[0057] (Embodiment 17) Fig. 25 to Fig. 26 are cross-sectional views in which a semiconductor integrated circuit device according to a sixteenth embodiment of the present invention is shown in order of the manufacturing process. In the embodiment 2, in the condition of Fig. 6, an aperture is provided in a protection insulating film 12, and the aperture is filled with metal films 65 and 66 whose main material is Al, then it is planarized and cleaned so as to share the surface with the protection insulating film 12. In addition, a thick polycrystalline Si film 24 is deposited on a semiconductor integrated circuit device formed on another single crystal Si substrate 11 by the same process as Fig. 6, and the surface is polished for planarization. Then, an adhesion layer 23 of a fluorine resin is formed on the surface, an aperture which reaches the semiconductor integrated circuit device is provided in the adhesion layer 23, and the side wall of the aperture is insulated. After that, the aperture part is filled with metal films 67 and 68 whose main material is Al, then it is planarized and cleaned so as to share the surface with the adhesion layer 23. After that, correct alignment is performed using the alignment equipment described above, and the two are bonded to each other (Fig. 25).

[0058] After that, the second Si substrate 11 is heated to 100 °C so as to melt the wax

20, and it is released from the quartz substrate 30, then the residual wax is cleaned and removed with acetone. And selective etching of the polycrystalline Si film 22 is performed. The wax removing process described above has no effect on the adhesion layer 23 which is formed of a fluorine resin. Next, on the single crystal ultra-thin film Si layer 1, a wiring 18 is made based on a desired circuit structure, so that a semiconductor integrated circuit device is completed (Fig. 26).

[0059] Memory cell arrays are laminated and integrated as a semiconductor integrated circuit device of the present embodiment, and the memory cell arrays in each layer are formed according to the same manufacturing process and the same heat treatment process, therefore they have the same function. The function is not affected by the lamination and integration at all. The maximum wiring length in a conventional planar structure integration construction is shortened by the lamination based on the present embodiment, and improvement in access rate is achieved. Furthermore, the present embodiment is a structure in which the connection wiring is exposed to the adhering surface and the connection wiring can be made on the exposed surface. Therefore, it is clear that the present embodiment has an advantage in which it can be easily applied to lamination of three or more layers by expanding the technique of the present embodiment.

[0060]

[Effect of the Invention] According to the present embodiment, semiconductor integrated circuit devices can be aligned extremely accurately and laminated in a longitudinal direction, so that further high integration of a semiconductor integrated circuit device can be realized, independently of increase in the area. As for the above-described lamination, semiconductor integrated circuit devices in each layer can be laminated, keeping exactly the same characteristics and the same function, including the heat treatment process. According to the present invention, an ultrahigh performance, high capacity semiconductor integrated circuit device which is required for next generation and more advanced generation can be manufactured using the semiconductor manufacturing equipment in being, without requiring the new equipment investment such as enlargement of a diameter of a semiconductor substrate. Furthermore, according to the present invention, a plurality of various semiconductor integrated circuit devices structuring a system can be halfway-manufactured beforehand, and the system wanted by customers can be manufactured speedily and shipped, corresponding to the demand situation. Therefore, shortening of the manufacturing process and reduction of the cost are achieved.

[0061] According to the present invention, basic circuits which structure

semiconductor integrated circuit devices can be manufactured on the same semiconductor substrate for each group of desired structure elements further, and an integrated circuit device can be made by integrating them on one basic circuit by the lamination. Therefore, the manufacturing process required for region separation and the occupied area can be omitted, compared to a conventional structure in which elements of different conductivity types are structured in the separated regions on the same substrate. In addition, restrictions on degree of freedom of element structure, based on mutual interference between adjacent elements and the manufacturing process of adjacent elements, can be resolved. By this, shortening of the manufacturing process and reduction of the cost are newly achieved.

[0062] Enlargement of the capacity and the area of a semiconductor integrated circuit device increases the percentage of defectively manufactured elements or structure circuits. However, according to the present invention, defective regions can be selected per element unit or desired unit, and the current path can be switched to the normal element or region on the structure circuit side. By this, non-defective yield of a semiconductor integrated circuit device of enlarged capacity and area can be greatly improved.

[0063] According to the present invention, in the manufacturing process of an ultra-thin film, when the ultra-thin film is transferred from a first support substrate to which the ultra-thin film is bonded to another support substrate, the first support substrate is released without consumption, so that a large scale semiconductor integrated circuit device can be manufactured at a low price.

[Brief Description of Drawings]

Fig. 1 is a cross-sectional view showing a conventional semiconductor integrated circuit device.

Fig. 2 is a cross-sectional view showing a manufacturing process of a semiconductor integrated circuit device of Embodiment 1 of the present invention.

Fig. 3 is a cross-sectional view showing a manufacturing process of a semiconductor integrated circuit device of Embodiment 1 of the present invention.

Fig. 4 is a cross-sectional view showing a manufacturing process of a semiconductor integrated circuit device of Embodiment 1 of the present invention.

Fig. 5 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 1 of the present invention.

Fig. 6 is a cross-sectional view showing a manufacturing process of a semiconductor integrated circuit device of Embodiment 2 of the present invention.

Fig. 7 is a cross-sectional view showing a manufacturing process of a

semiconductor integrated circuit device of Embodiment 2 of the present invention.

Fig. 8 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 2 of the present invention.

Fig. 9 is a cross-sectional view showing a manufacturing process of a semiconductor integrated circuit device of Embodiment 3 of the present invention.

Fig. 10 is a cross-sectional view showing a manufacturing process of a semiconductor integrated circuit device of Embodiment 3 of the present invention.

Fig. 11 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 3 of the present invention.

Fig. 12 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 4 of the present invention.

Fig. 13 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 5 and 6 of the present invention.

Fig. 14 is a cross-sectional view showing a manufacturing process of a semiconductor integrated circuit device of Embodiment 7 of the present invention.

Fig. 15 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 7 of the present invention.

Fig. 16 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 8 of the present invention.

Fig. 17 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 9 and 10 of the present invention.

Fig. 18 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 11 of the present invention.

Fig. 19 is a cross-sectional view showing a manufacturing process of a semiconductor integrated circuit device of Embodiment 12 of the present invention.

Fig. 20 is a completed cross-sectional view of a semiconductor integrated circuit device of Embodiment 12 of the present invention.

Fig. 21 is a schematic diagram showing manufacturing equipment of a semiconductor integrated circuit device of Embodiment 13 of the present invention.

Fig. 22 is a schematic diagram showing manufacturing equipment of a semiconductor integrated circuit device of Embodiment 13 of the present invention.

Fig. 23 is a cross-sectional view showing a manufacturing process of a semiconductor integrated circuit device of Embodiment 15 of the present invention.

Fig. 24 is a plan view showing a semiconductor integrated circuit device of Embodiment 16 of the present invention.

Fig. 25 is a cross-sectional view showing a manufacturing process of a

semiconductor integrated circuit device of Embodiment 17 of the present invention.

Fig. 26 is a plan view showing a semiconductor integrated circuit device of Embodiment 17 of the present invention.

Fig. 27 is a cross-sectional view showing an example of a conventional semiconductor integrated circuit device.

[Description of Symbols]

1: semiconductor substrate
2: insulating film for isolation between elements
3: gate insulating film
4 and 5: gate electrode
6, 7 and 8: diffused layer
9 and 15: terminal electrode
10: electrode protection insulating film
11: semiconductor substrate
14: wiring
16: protection insulating film
17: connection wiring
18: wiring
19: gate electrode
20 and 25: wax
21 and 23 adhesion layer
22, 24, 27 and 28: polycrystalline Si film
26 and 29: adhesion layer
30: transparent quartz substrate
31, 35 and 40: Si substrate
32: thin insulating film
33: low resistance polycrystalline Si film
36: thermally-oxidized film
37: low resistance conductive wiring
38: polycrystalline Si film
39: electrically open region
41 and 44: electrode protection insulating film
42 and 43: low resistance conductive film
45: adhesion layer
46 and 47: gate electrode
49: electrode

50: ultra-thin film Si layer where a main storage is structured

51, 52 and 53: ultra-thin film Si layer where an extended storage is structured

54: ultra-thin film Si layer where a central processor is structured

55 and 56: gate electrode of a transistor for current path control

57 and 58: ultra-thin film semiconductor integrated circuit device

59: through-hole

61, 62 and 63: diffused layer

71, 72 and 73: stage

74: block

75 and 76: substrate

77, 78 and 84: position detecting optical system

79: position perception part

80 and 81: stage mark

82: substrate deformation control mechanism

83: computer control control system

85: stage position control system

86: movement mechanism

201: first semiconductor integrated circuit layer

202: second semiconductor integrated circuit layer

203: insulating film

205: interlayer wiring

211: first wiring layer

221: second wiring layer

212: first active layer

222: second active layer

213: gate electrode of a first layer